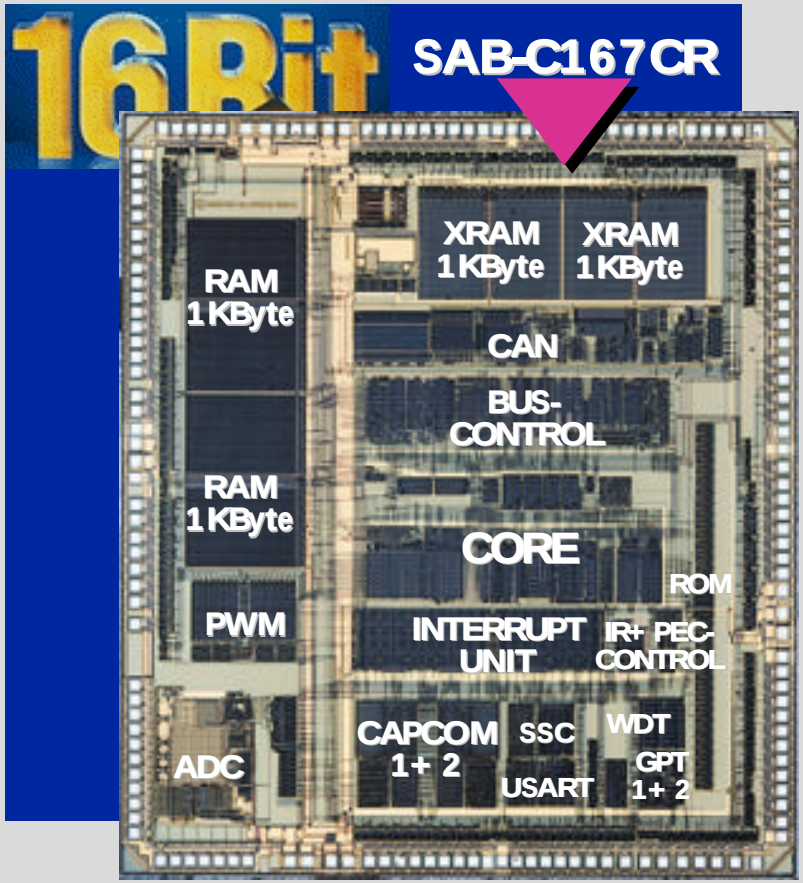
C166 Family-High Performance 16-Bit Microcontrollers



- SAB 8xC166
- C167x
- C165
- C163
- C164x
- C161x

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C166 Family
The Three Subsystems

C161
C163
C164
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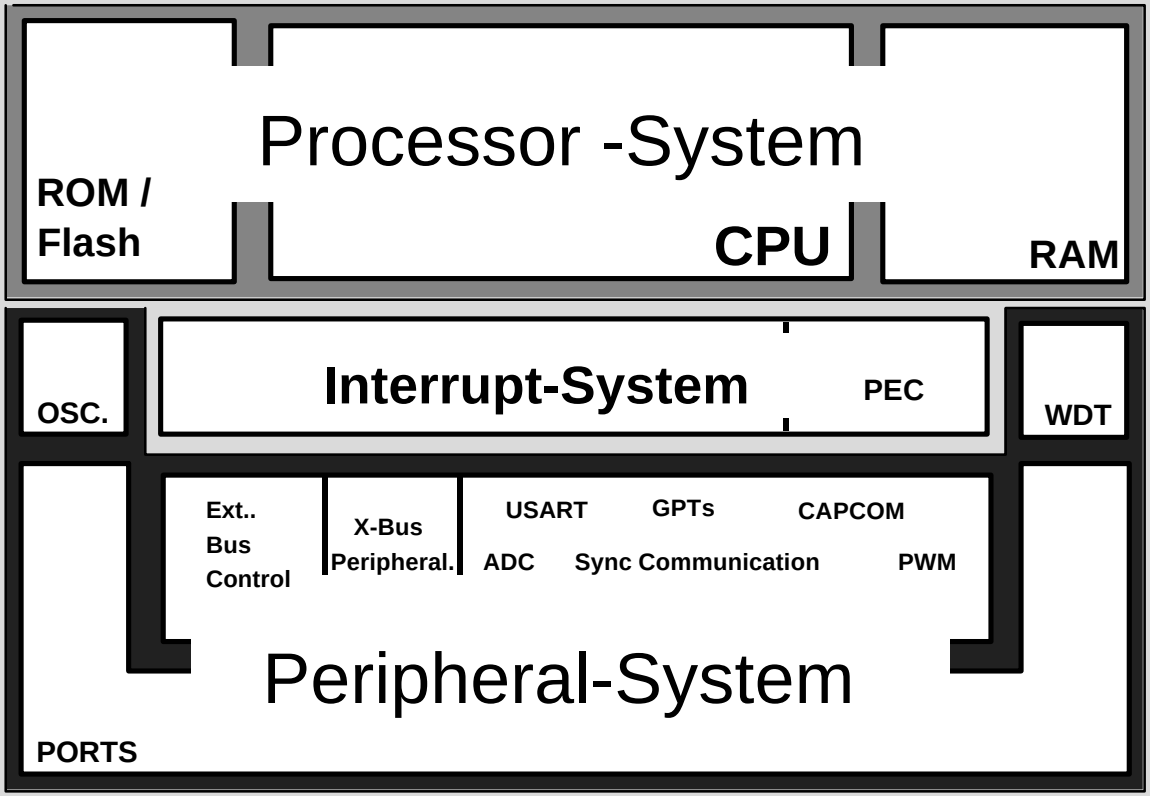
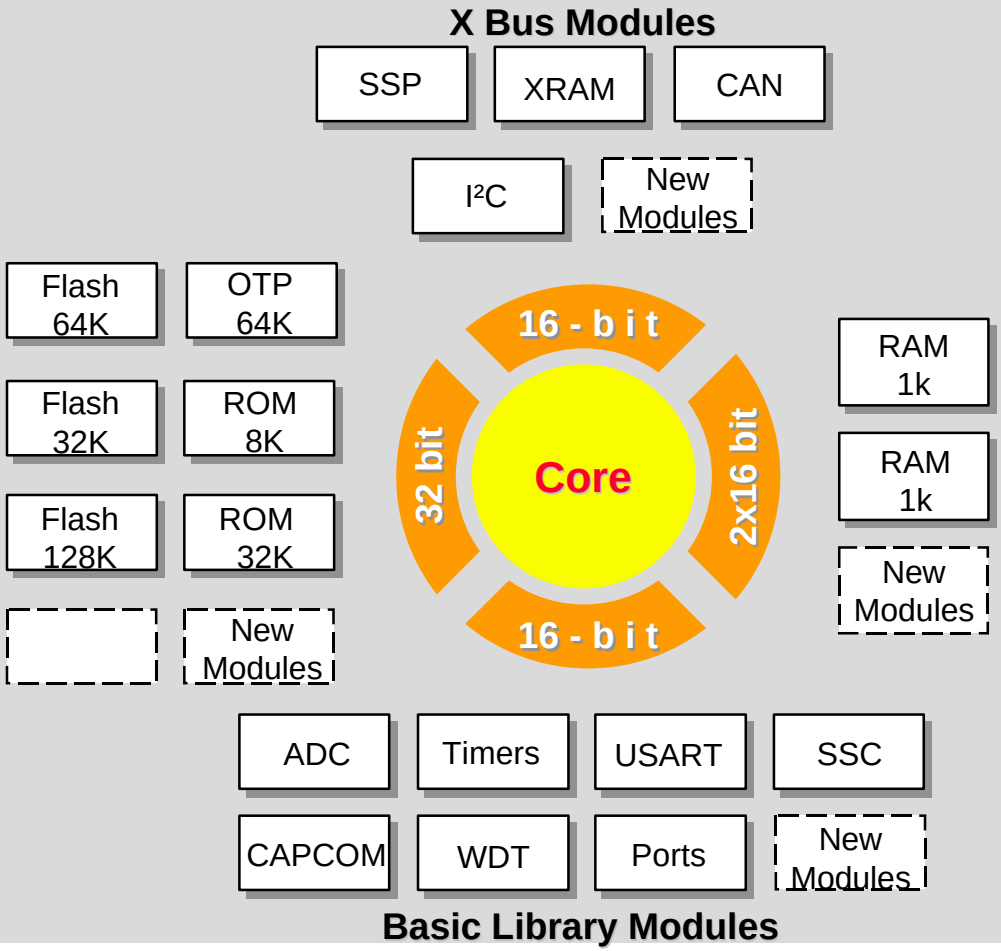
C167



Four Bus Modular System



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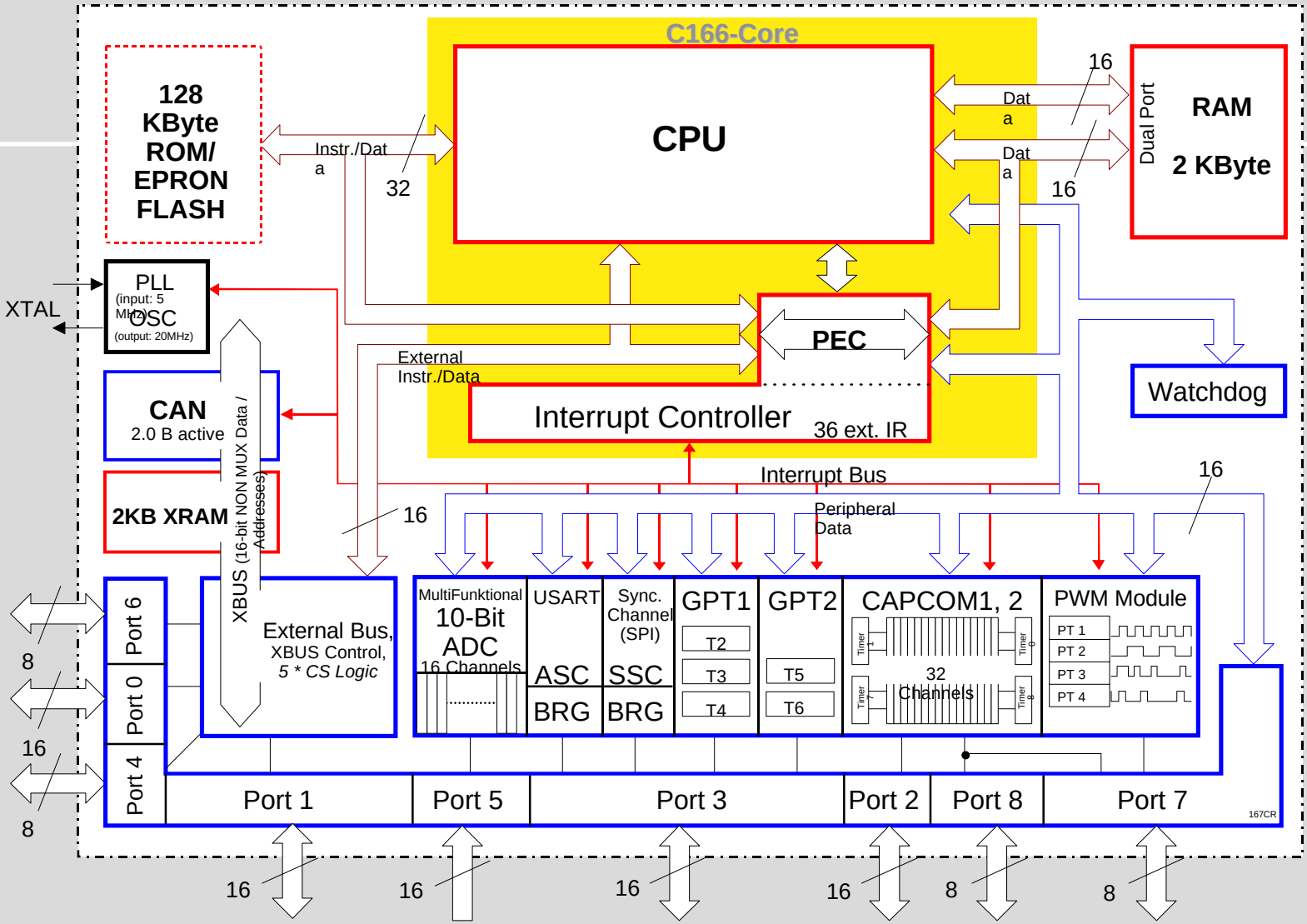

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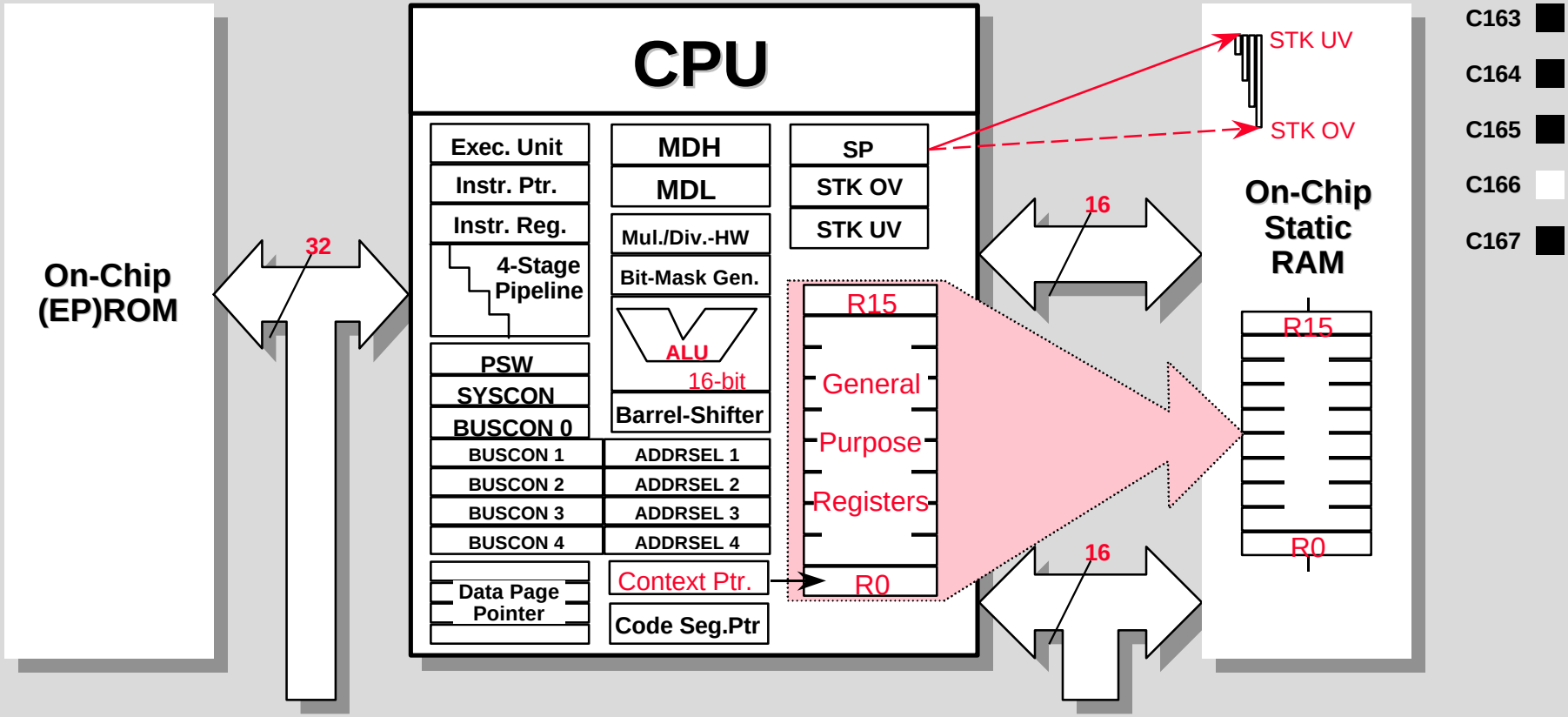
Overview - C167CR Block Diagram

Microcontrollers

Block Diagram
ROM / RAM interaction



General Purpose Register (GPR)

- **Up to 16 GPRs = 1 Register bank Consisting of max.**
  - 8 Word-Registers
  - 8 Word-Registers with lower and higher Byte access
- **The GPRs are bit-addressable**
- **Any Register bank can be freely allocated in internal RAM**
- **The location of the active Register bank is determined by Context Pointer (CP)**
- **CP can be easily switched, to select another Register bank**
- **SWTC (one instruction cycle)**

C161 ■
C163 ■
C164 ■
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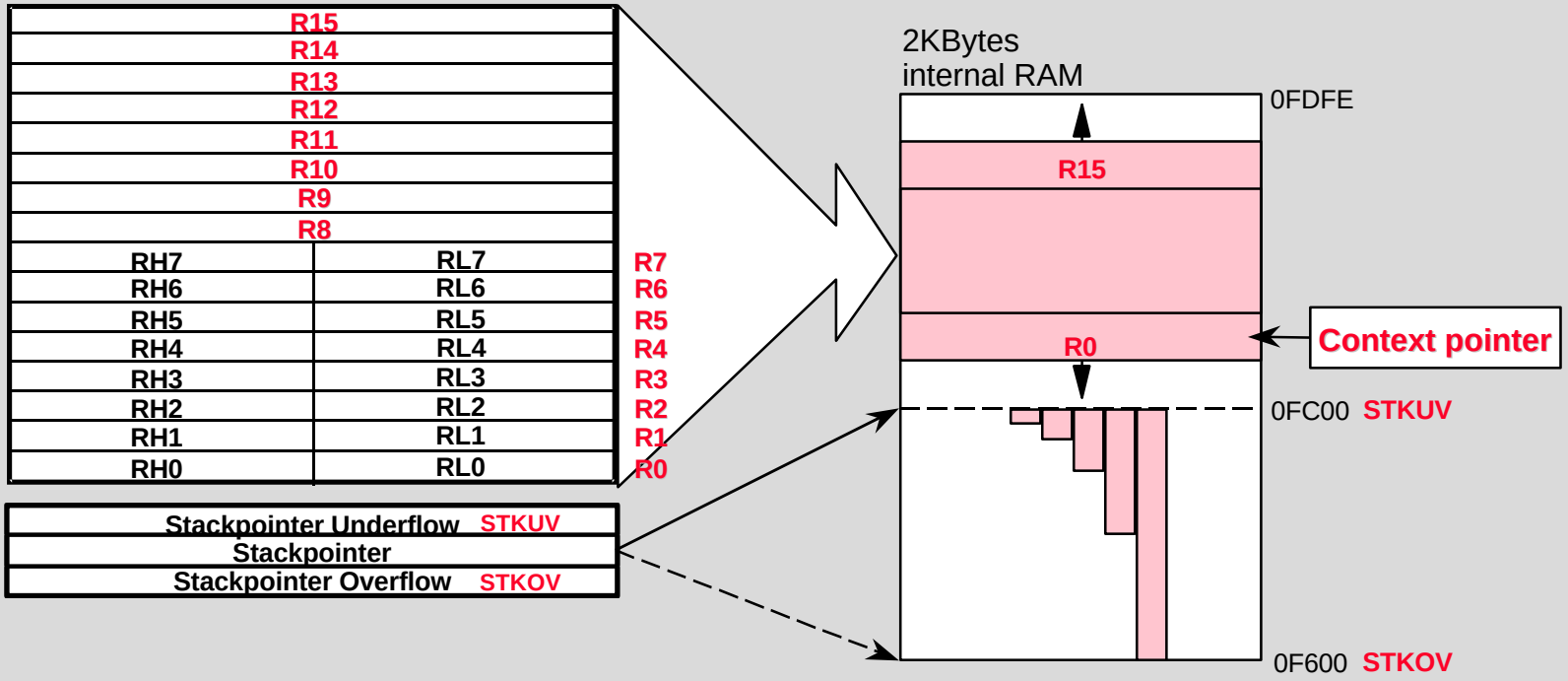
Block Diagram
ROM / RAM interaction with 2K RAM



Four Stage Instruction Pipeline at 20 MHz

- **Effective execution time of most instruction in 100 ns**
- **Three word prefetch queue (buscontroller) to support pipeline**
- **Optimized branch processing**
  - For branch instruction (Jump, Cond. Jump, Call, Return,...) only one additional machine cycle is normally required to fetch target instruction
- **Jump Cache**
  - For loop processing no additional machine cycle is required

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Four Stage Instruction Pipeline at 20 MHz

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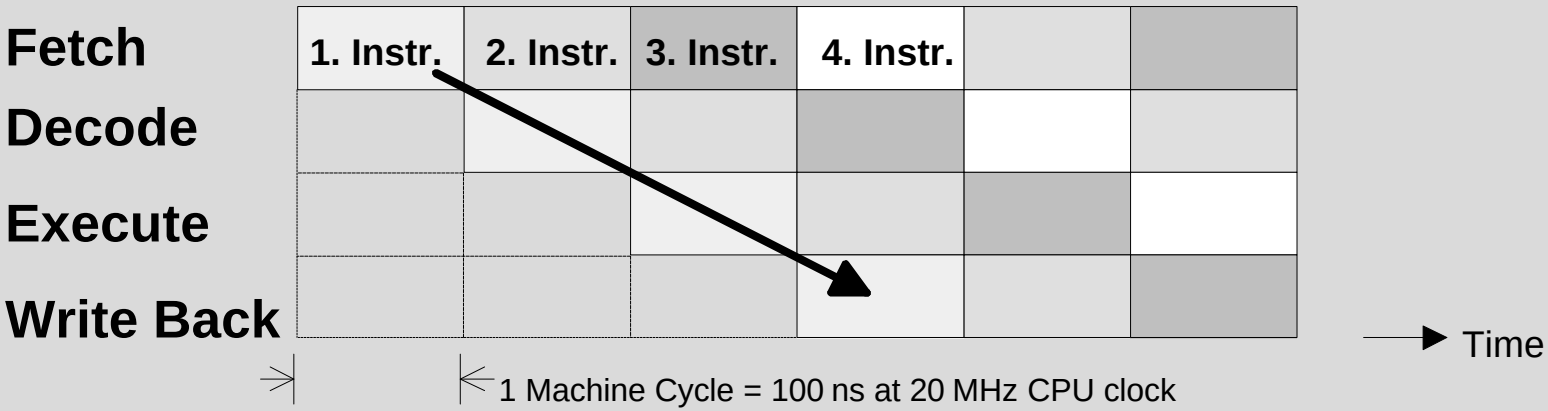
Processing of each instruction is partitioned in 4 stages



Instruction Set at 20 MHz

- **Data manipulation**
  - Arithmetic and boolean instruction incl. fast multiply/divide in 0.5/1.0us
  - Multiple (up to 15) bit shift and rotate in 100 ns
  - Bit to bit manipulation in internal RAM and SFR's
- **Data movement**
  - MOV instructions with all important addressing modes
  - Byte to word conversion
  - System stack (PUSH, POP) with over- and underflow control
  - User stack (MOV with auto increment and decrement)
- **...**

C161 □
C163 □
C164 ■
C165 □
C166 ■
C167 ■

...Instruction Set at 20 MHz

- **Program manipulation**
  - Jumps and calls / conditional jumps under 16 different conditions
  - Software- and hardware-Traps
  - Fast context switching in 100 ns

- **Special instructions for**
  - Power consumption reduction and system Control
  - Non-interruptable instruction sequences
  - Extended addressing access

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C164 ■
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C167 ■

Address Space...

- **Complete address space**
  - "von Neumann" architecture with multiple internal bus structure to avoid bus bottlenecks
  - 64KByte non-segmented address space
  - up to 16 MBytes
  - segmented address space: 64KB code segments and 16K data pages

- **Internal address space**
  - up to 128 KBytes ROM / Flash-EPROM
  - max 4 KByte SFR's

	C167	C167CR
RAM	4 KByte	4 KByte
ROM	128 KByte Flash	128 KByte Flash

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C167

...Address Space

- **Flexible ext. bus configurations to simplify system integration**
  - up to 24-bit Address / 8-bit Data (MUX and NMUX)
  - up to 24-bit Address / 16-bit Data (MUX and NMUX)
  - Five completely independent configuration registers
  - Five programmable chip selects and programmable bus control signal to save external glue-logic
  - Programmable HOLD/HOLDA/BREQ bus arbitration function for multi-master operations

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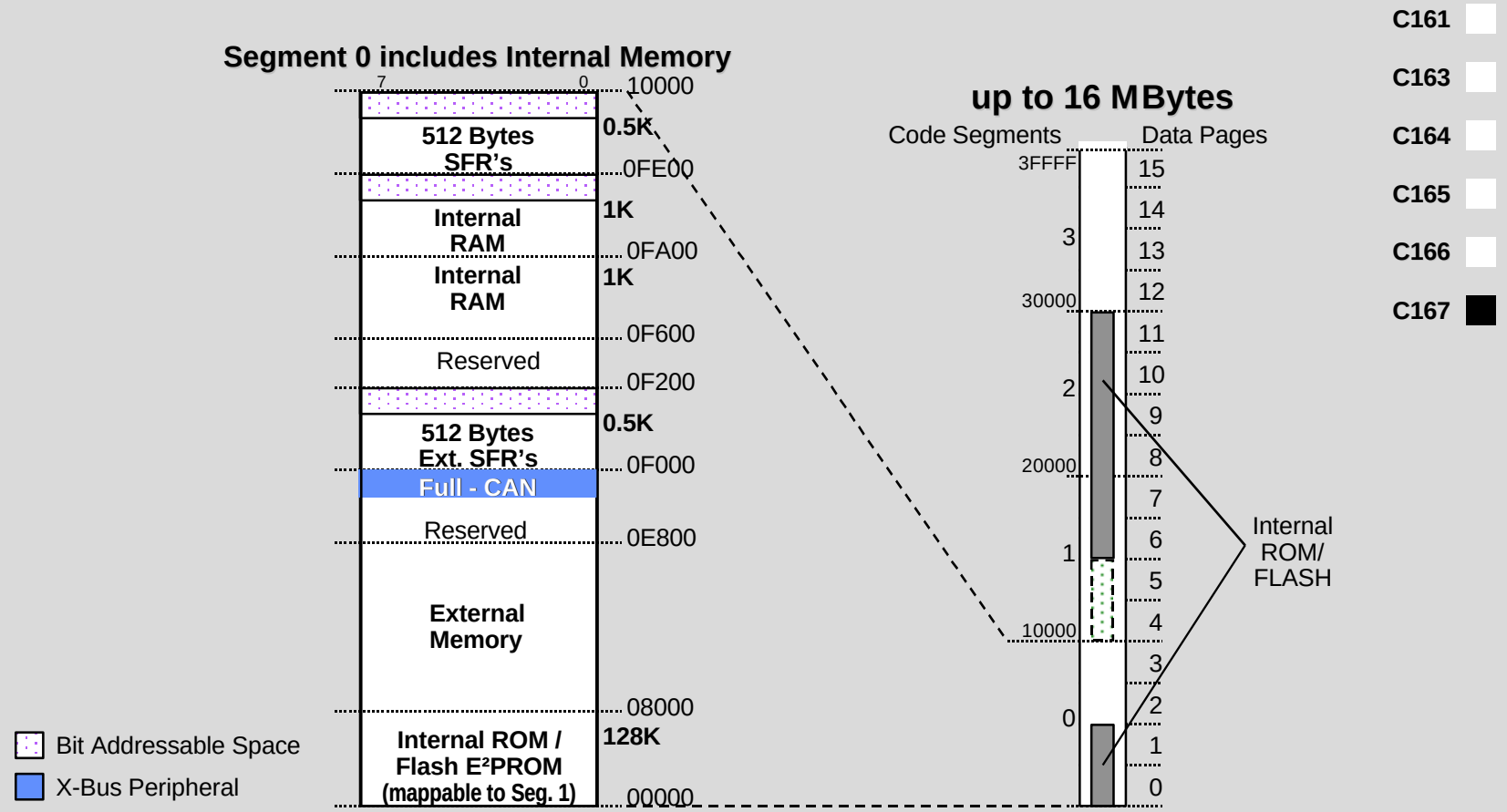
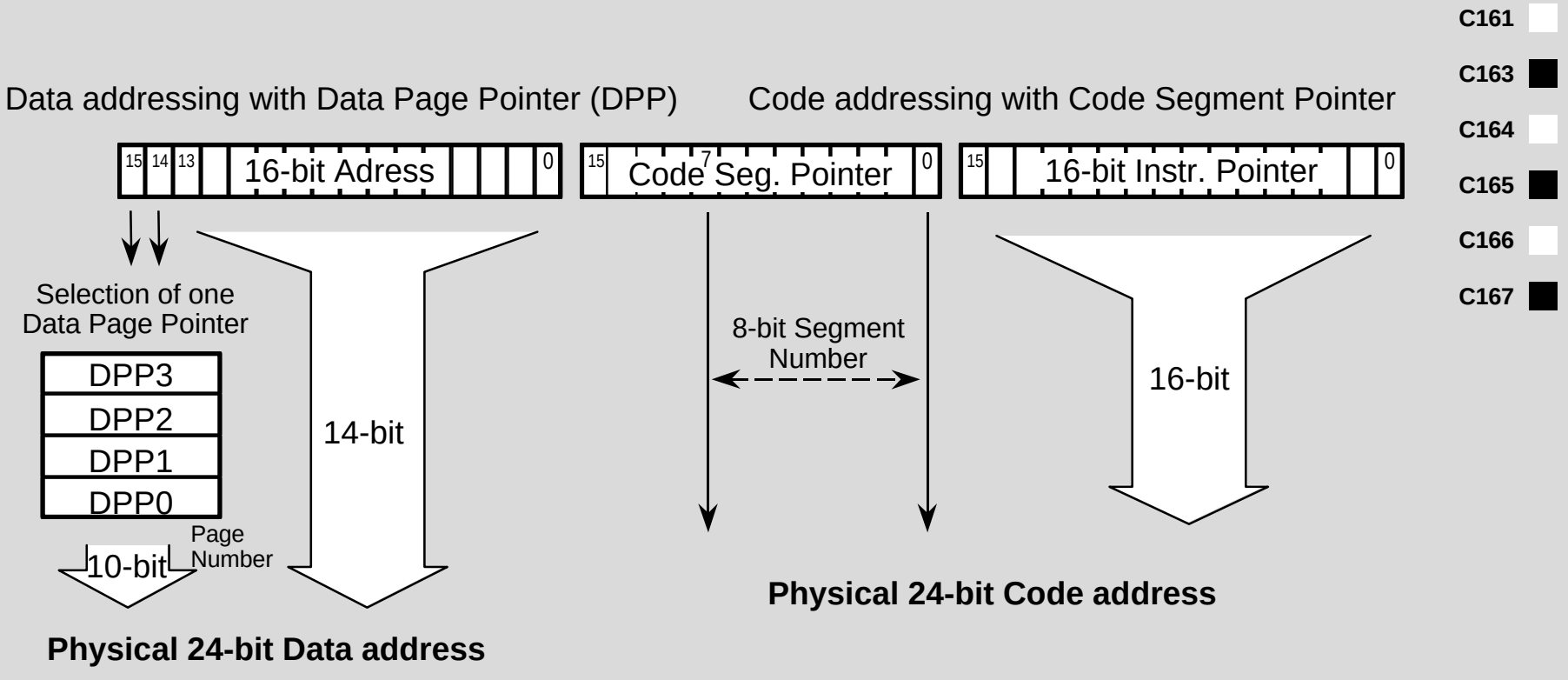
C163 ■
C164 ☐
C165 ■
C166 ☐
C167 ■

Internal and external Memory Map - C167CR



Code and Data Addressing via Segmentation and Paging on 16 Mbyte address range



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Data Addressing via Data Page Pointer (DPPx)

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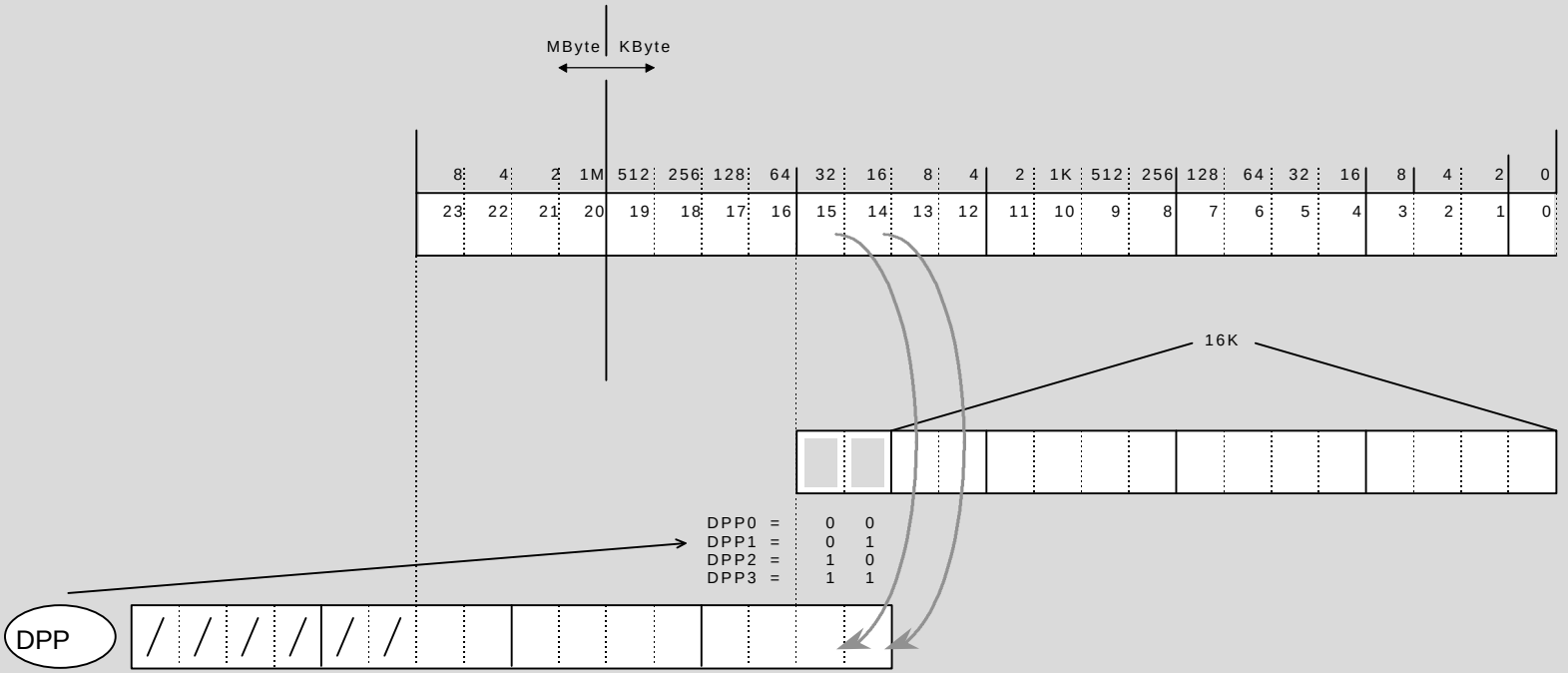


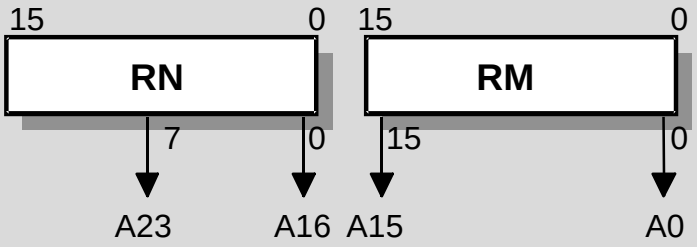
Data Addressing via Extended Mode

- **Overrides standard DPP addressing scheme to ease large (up to 32-bit) address calculation**
  - Segment or Page override by an immediate value
  - Segment and Page override by a Register contents

C161 ■
C163 ■
C164 ■
C165 ■
C166 □
C167 ■

Examples: **Override Segment Number**

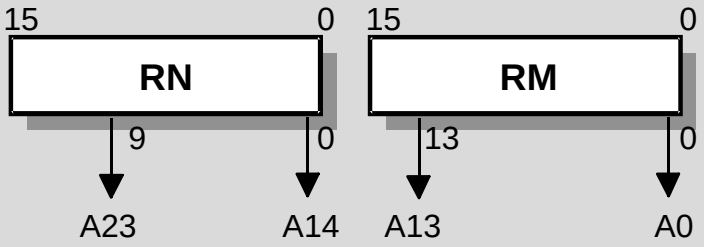
```
EXTS RN,#data2 ;data2:No. of instructions
MOV [RM],Ri    ;to be used for Ext.Addr.Mode
```



Physical address, where the contents of Ri is moved to

Override Page Number

```
EXTP RN, #data2
MOV [RM], Ri
```



Physical address, where the contents of Ri is moved to

Overview at 20MHz...

- **Interrupt Controller**
  - Extremely short interrupt response time of minimal 250ns typical: 400ns
  - Interrupt execution in small time segments
  - Ensures highest real-time performance
  - Comprehensive prioritization scheme
    - **Easy scheduling of complex real-time systems by using up to 64 priority levels (4 groups within 16 levels)**
  - Non-maskable interrupt input (NMI)
  - Hardware-Traps on runtime errors and Software-Traps
- **...**

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...Overview at 20MHz

- **CPU independent interrupt-service via Peripheral Events Controller (PEC)**
  - Off-loads the CPU from simple but frequent interrupt-services
  - Interrupt-driven “DMA-like” data transfer to any location in segment 0, without task switch of the CPU
  - Makes peripheral data transfers Independent of running CPU routine
  - Response-time is minimal 150ns, typical 300ns with a CPU load of 100ns

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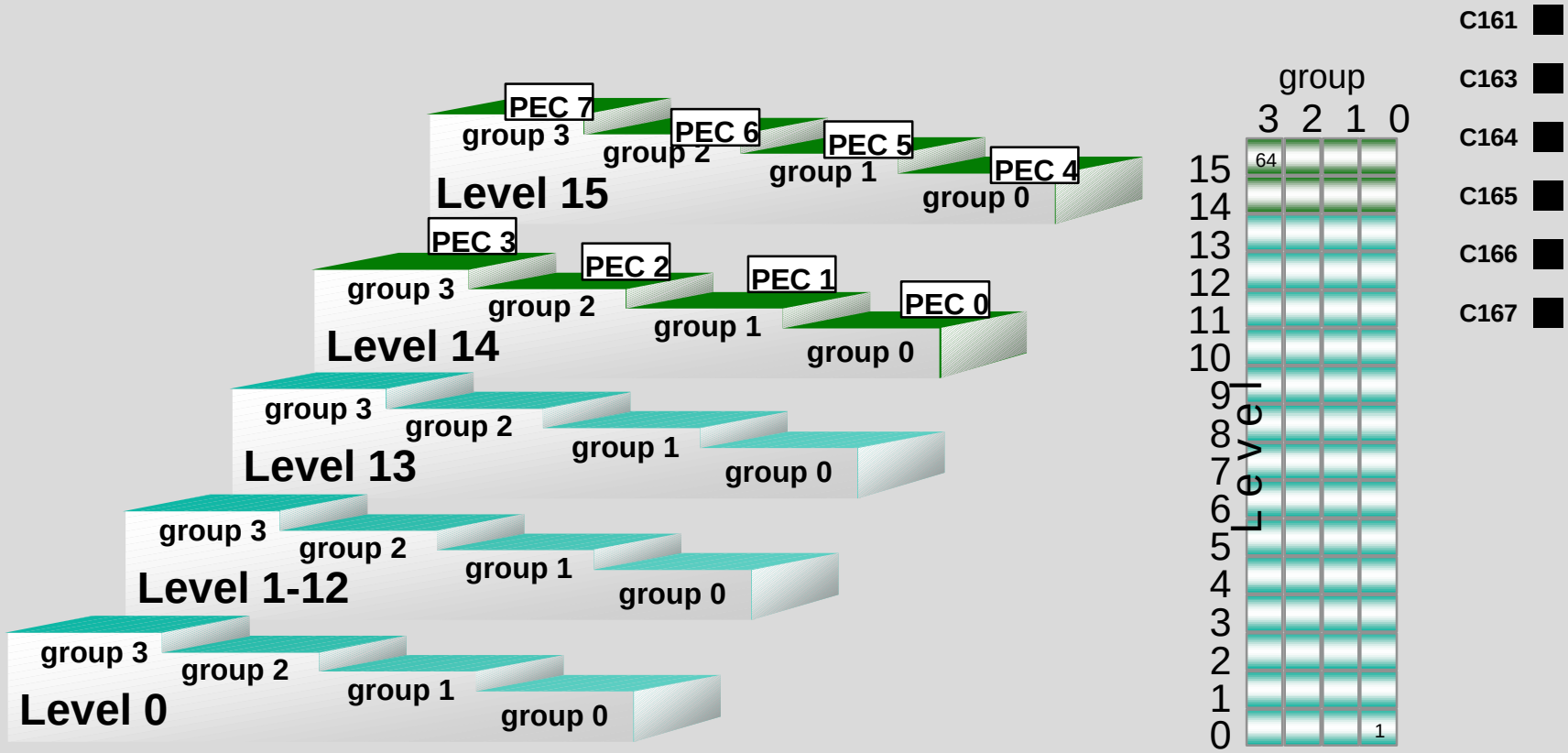
C163 □
C164 ■
C165 □
C166 ■
C167 ■

Priority System, PEC



Interrupt Processing

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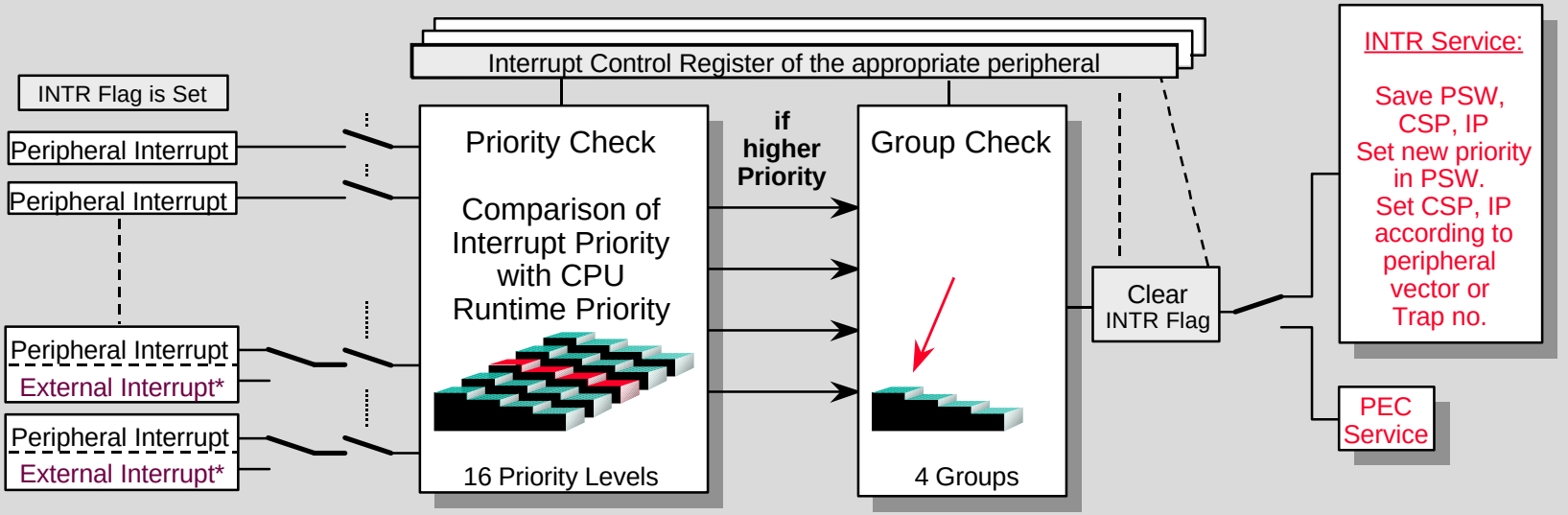
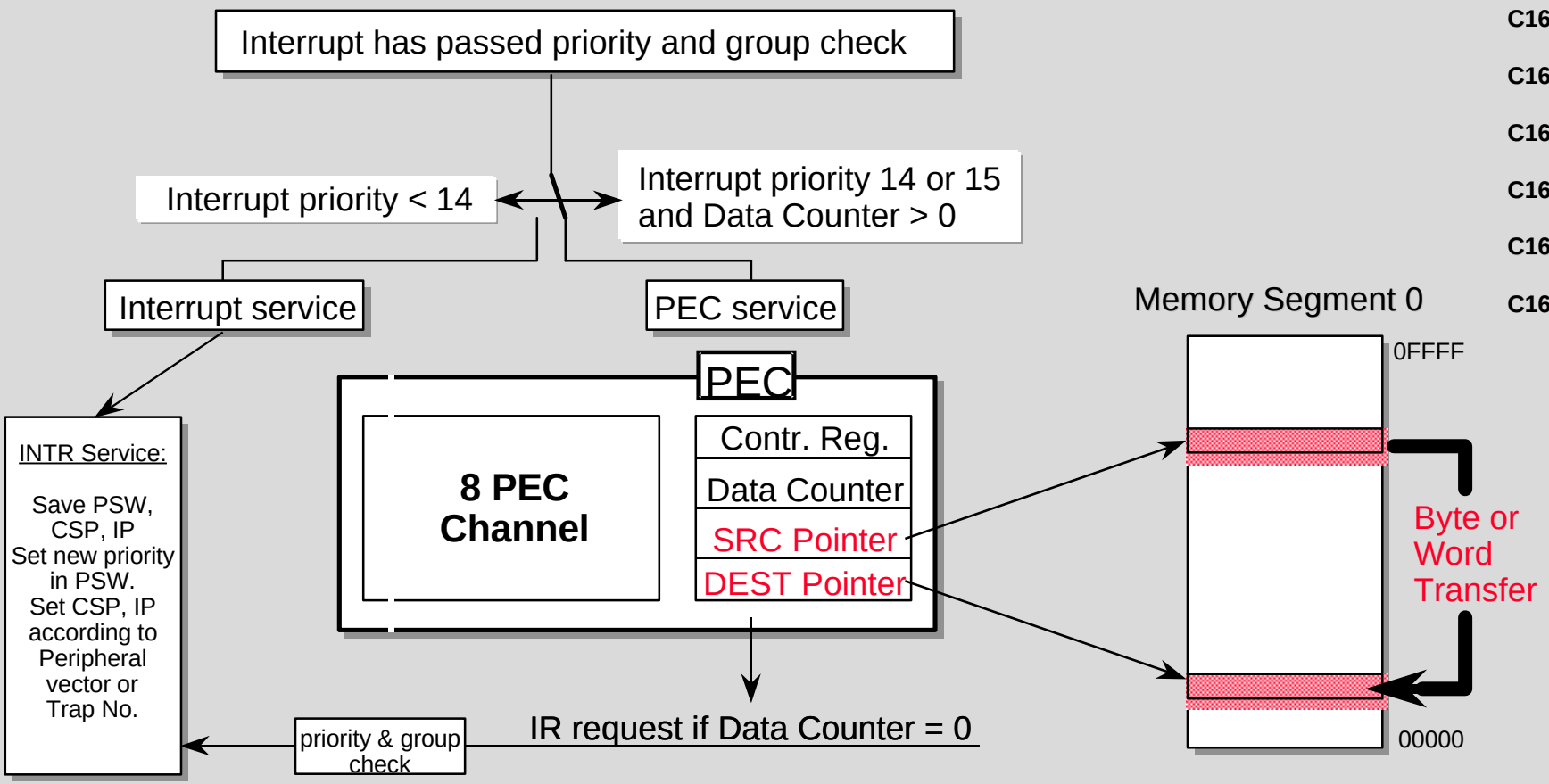


*** External Interrupts are possible, e.g. instead of the Capture Input**

55 Peripheral Interrupts

36 ext. Interrupts(+ NMI) including 8 which are sampled every 50 ns

Peripheral Event Controller (PEC)



Peripherals Set of the C167...

- **2 General Purpose Timer units (GPT1 & GPT2)**
  - 5 Timers (200/400ns) with enhanced Input/Output, Reload and Capture functions and complex concatenation capabilities
- **2 Capture/Compare units (CAPCOM1 & 2)**
  - 4 Timers (400ns) with Reload register and 32 independent 16-bit Capture/Compare channels programmable to 6 modes of operation
- **4 high resolution PWM channels**
  - each with independent time-base of up to 50ns resolution and programmable operation modes (edge-aligned, center-aligned, burst and single-shot mode)
- **...**

C161
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C167

...Peripherals Set of the C167

- **Independent USART**
  - max 625 KBaud asynchronous and max 2.5 Mbit/sec synchronous data transfer
- **Fast Serial Synchronous Communication interface (SSC)**
  - max 5 Mbit/sec full duplex transfer rate, SPI compatible
- **Fast and accurate A/D Converter**
  - 10-Bit resolution, 16 input channels, 9.7µs conversion time, enhanced continuous and scan modes with channel-injection capability.
- **I/O Ports**
  - 8 Ports provide 111 I/O lines
- **Watchdog: 16-Bit Reload-timer causes reset on overflow**

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C167

General Purpose Timer 1(GPT 1) at 20 MHz

- **Three 16-bit up/down timers: 2 auxiliary timers(T2,T4) and 1 core timer(T3)**
- **Input mode**
  - Timer mode: Internal clock input with prescaler up to 2.5 MHz / 400 ns; Clock can be gated with external signal
  - Counter Mode: external clock up to 1.25 MHz
  - Cascading of core timer and any aux. timer (33-Bit timer)
- **Count direction (only T3) can be changed externally**
- **Output mode**
  - Interrupt possibility and toggle function at the core timer T3
  - Interrupt possibility at auxiliary timers T2 and T4
- **Reload: Core timer can be reloaded with the contents of any aux. timer**
- **Capture: Contents of the core timer can be latched into any aux. timer**

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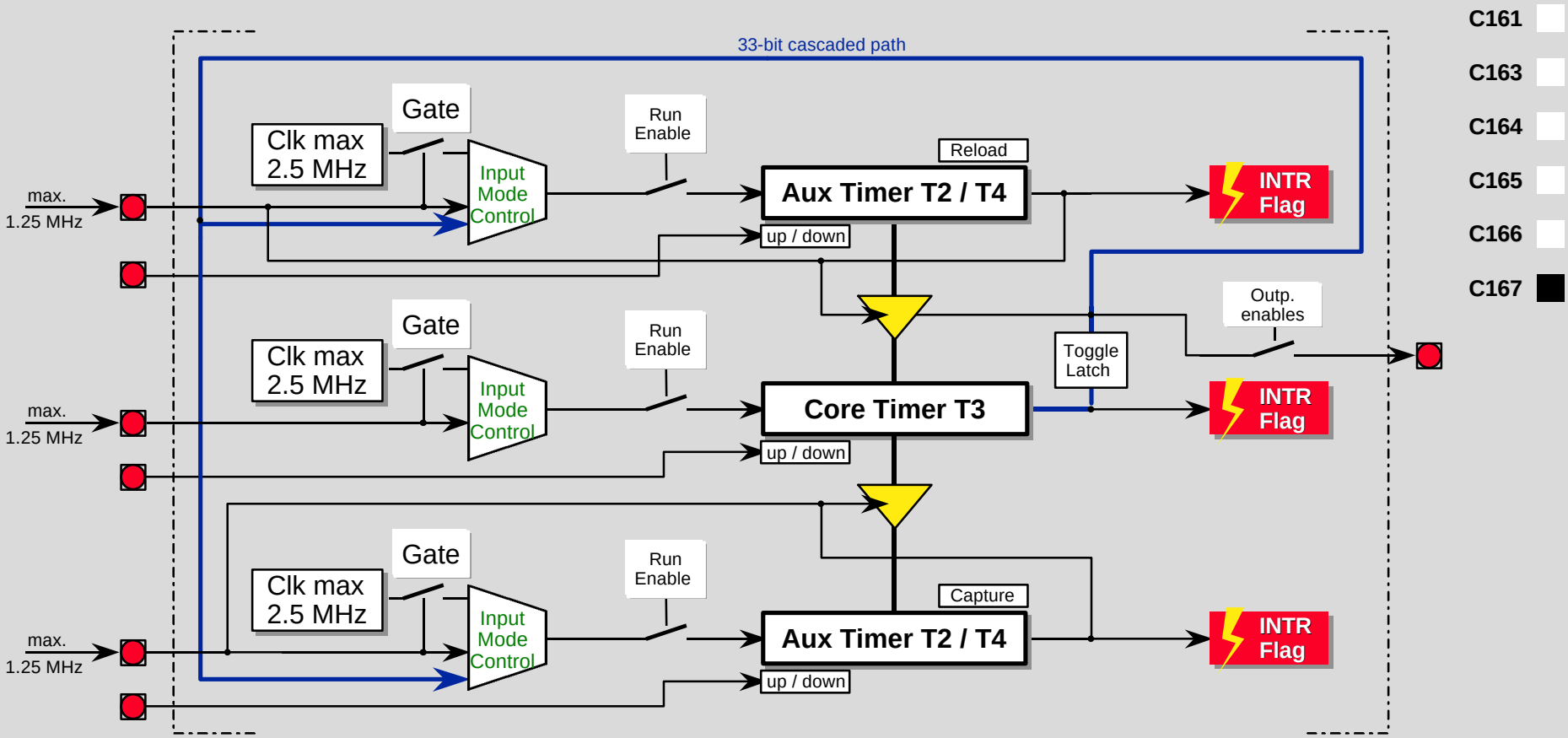
GPT 1 Function Diagram at 20 MHz



General Purpose Timer 2 (GPT 2) at 20 MHz

- **Two 16-Bit up/down timers (T5, T6)**
- **Input mode**
  - Timer mode: Internal clock input with prescaler up to 5MHz (200ns)
  - Counter mode: External clock up to 2.5 MHz
  - T5 can also be clocked with the toggle bit of T6
- **Output mode**
  - Interrupt possibility and toggle function of a port line (via a toggle bit)
  - Output of T6 can be used to clock CAPCOM timers
- **Count direction of all timers can be dynamically changed (C167)**
- **Cascading of timer T6 with timer T5**
- **One 16-Bit Capture(for T5) / Reload(for T6) register**
  - Reload register for T6, Capture register for T5

C161 ☐
C163 ☐
C164 ☐
C165 ☐
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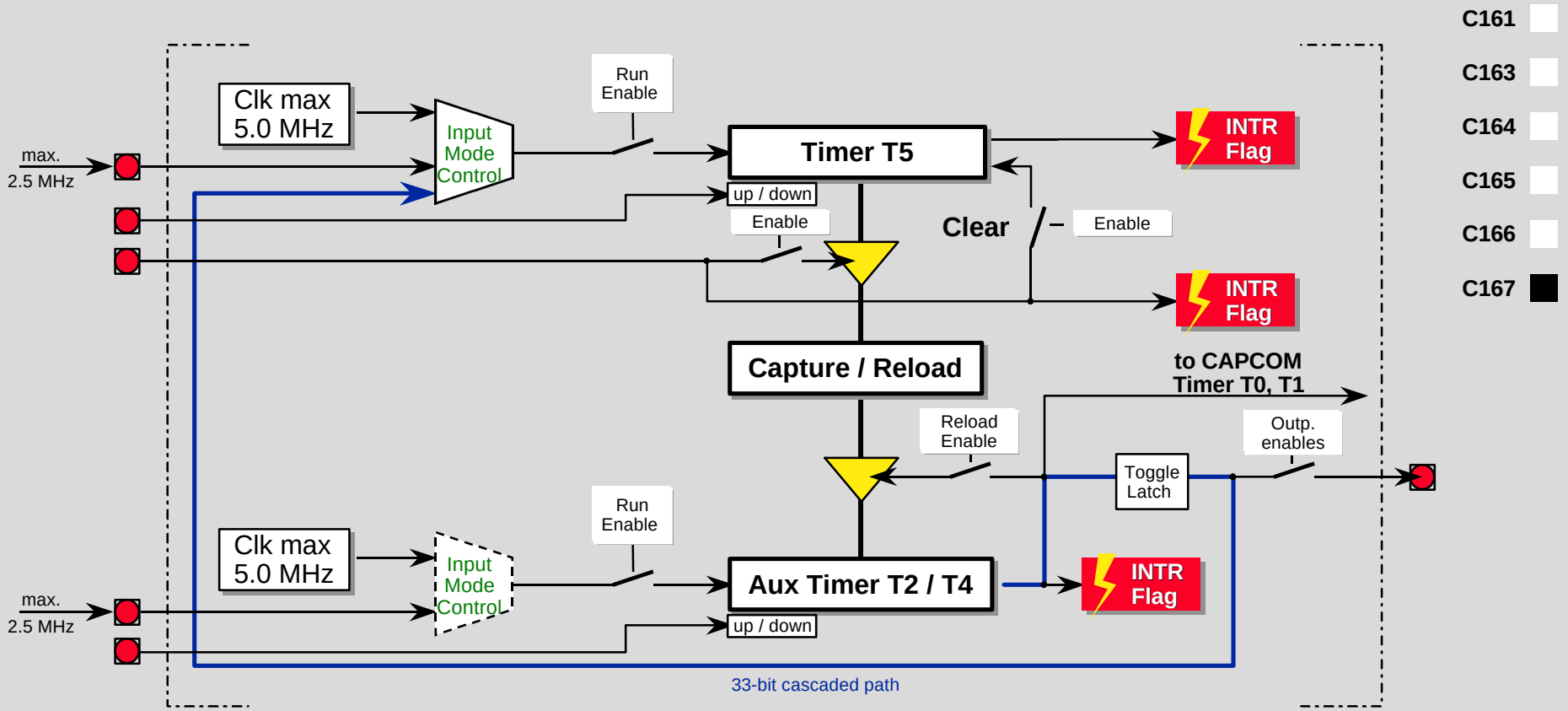
C167 ■

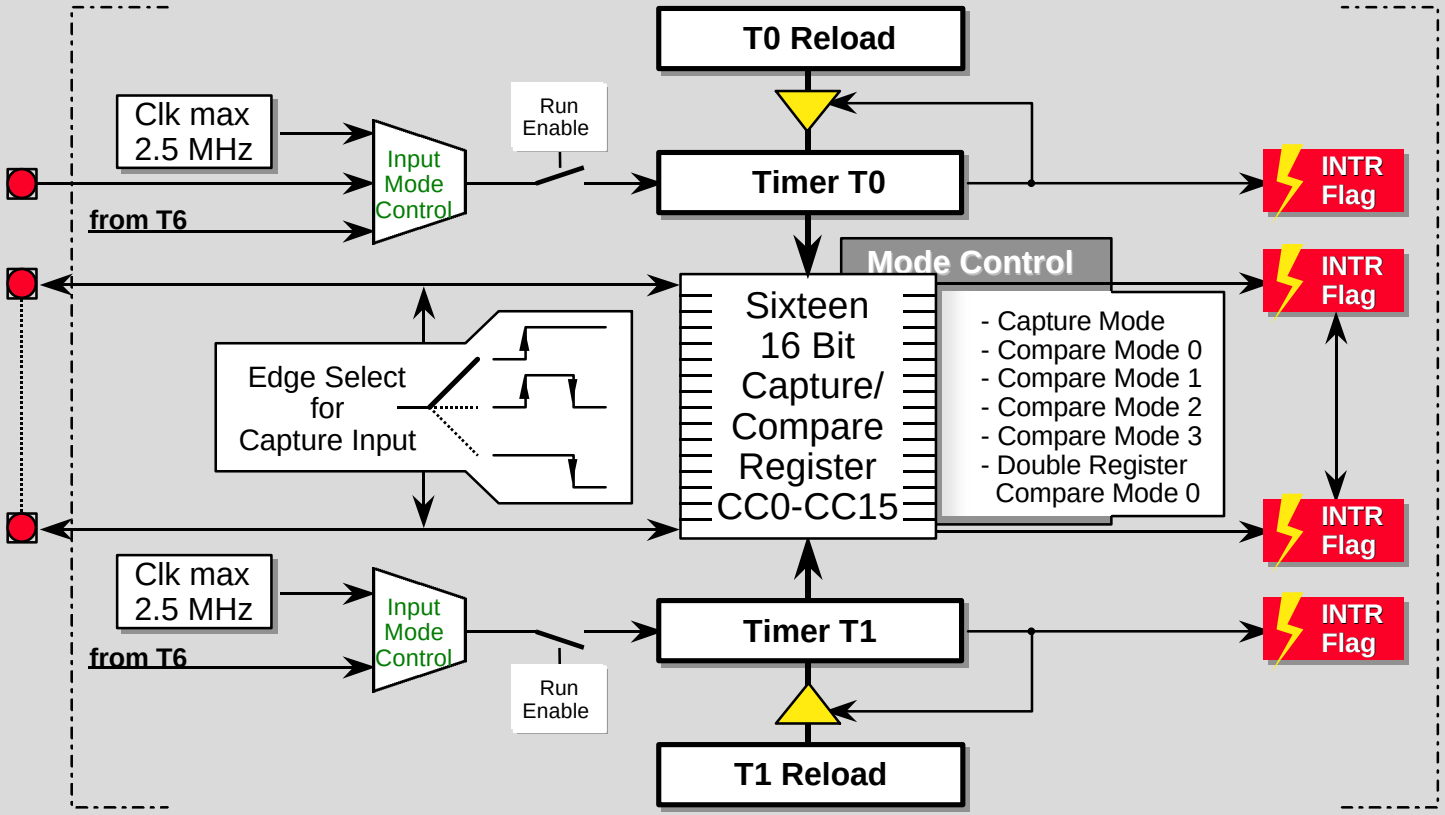
GPT 2 Function Diagram at 20 MHz



Capture / Compare Unit 1/2 (CAPCOM 1/2)...

- **Four 16-bit timers (T0/T1 & T7/T8), 16-bit reload reg. each**
  - **Timer mode:** Int. clock input with up to 2.5 MHz (400ns)
  - **Counter mode:** External clock input to T0/T7 up to 1.25 MHz, Output from T6 can be used as clock input
  - CAPCOM 2 can be synchronized via T0 to CAPCOM 1
- **Two units with sixteen 16-Bit Capture/Compare registers**
  - Individually program. for Capture or any Compare mode
  - Individually allocatable to timer T0/T1 or T7/T8
- **Various Compare modes for flexible Pulse Width Modulation(PWM)**
  - Output-Pin toggles if Compare is true
  - 1 or 2 Compare registers can operate to one Output-Pin
  - One or more Compare events can be detected in one timer period
  - Interrupt only mode

CAPCOM(1)
Function Diagram



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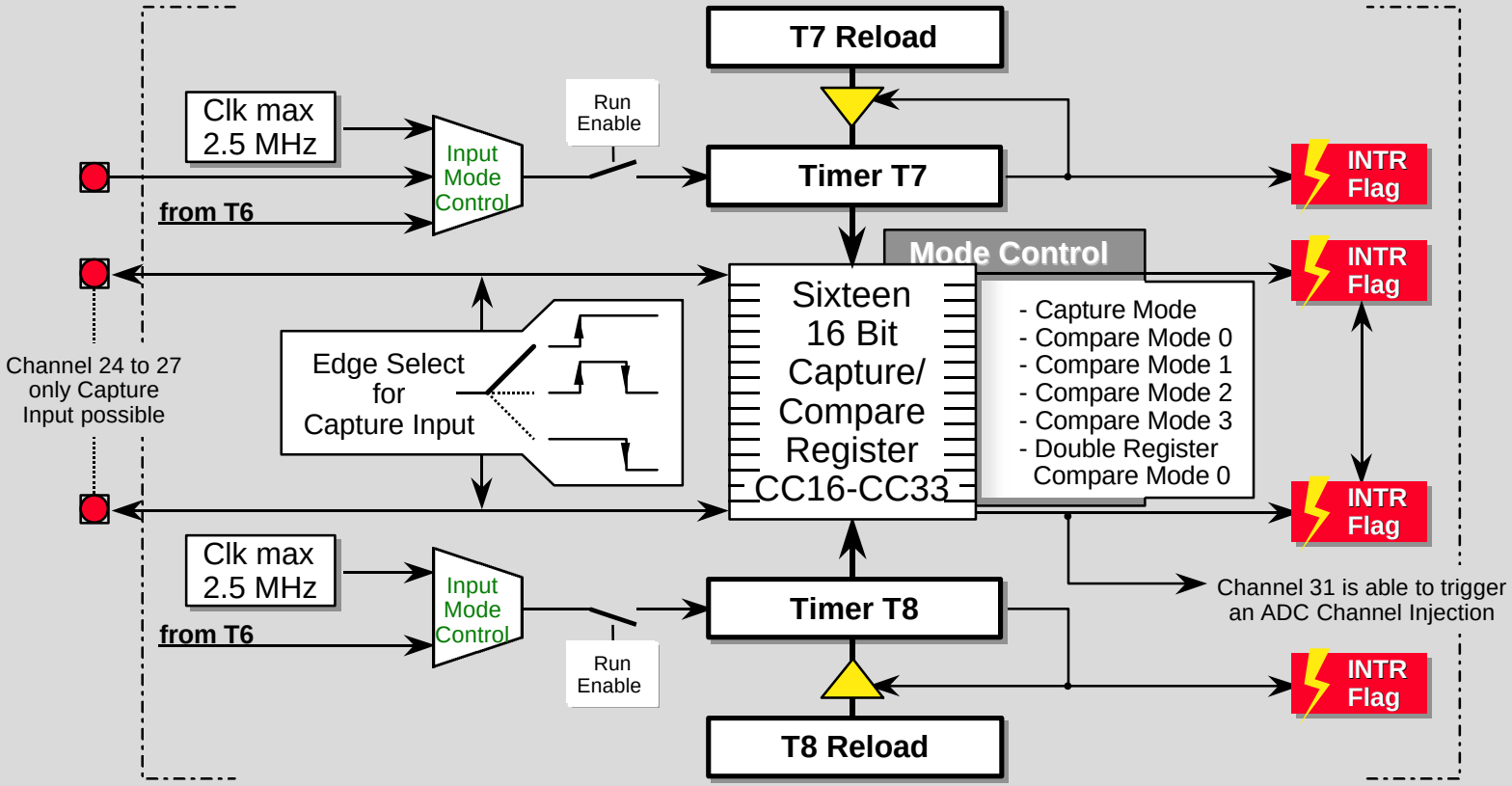
CAPCOM 2
Function Diagram



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CAPCOM 1/2
Compare Mode 0 and 1

- **Several Compare events are possible within a single Timer period**

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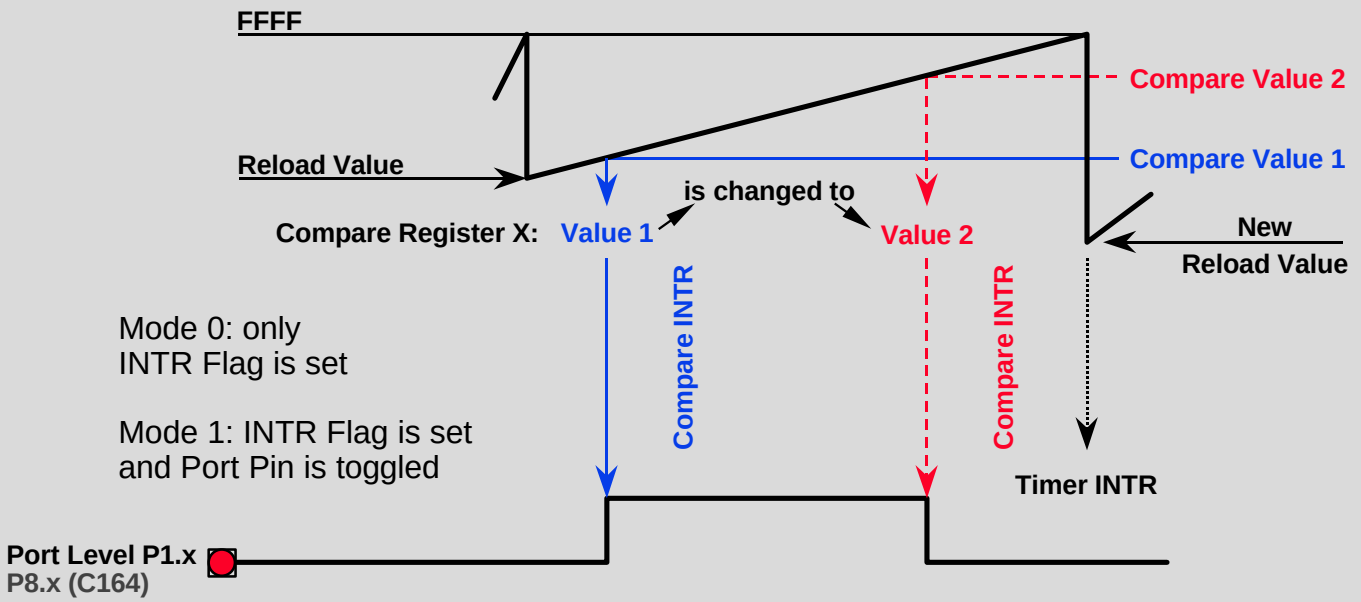

CAPCOM 1/2
Compare Mode 2 and 3

- **Only one Compare events is possible within a single Timer period**

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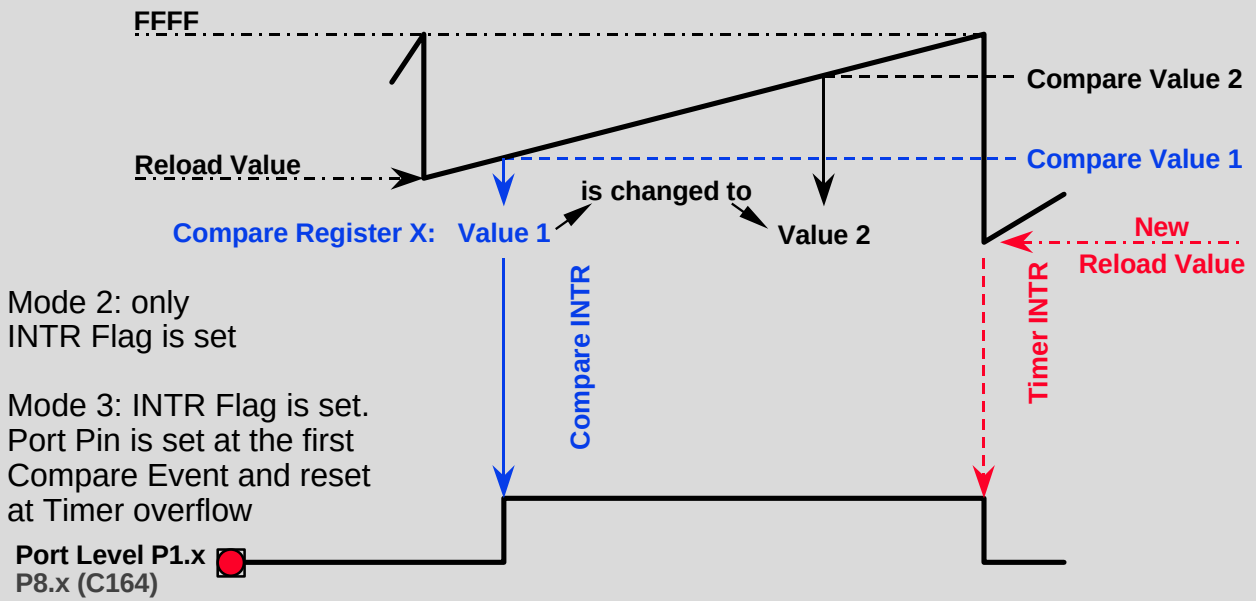

CAPCOM 1/2
Double Register Compare Mode

- **Two Compare Register work together to control one Port Pin**
- **This mode is selected by a special combination of the mode 0 and 1**

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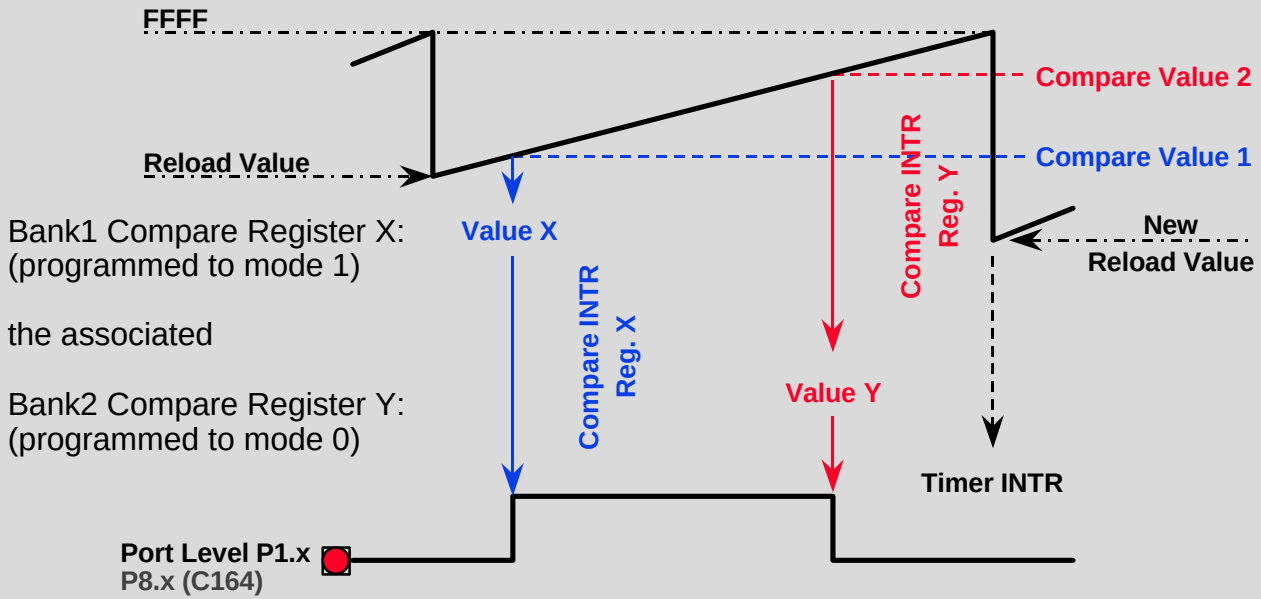

Pulse Width Modulation Unit (PWM)

- **4 completely indep. PWM channels each with its own time-base**
  - 50ns or 12.8µs timer-resolution provides a very wide frequency range to generate PWM signals
  - Programmable output polarity
  - Up to 78 KHz at 8-bit PWM resolution

$$F_{PWM} = \frac{1}{2^{8\text{-bit}} \times 50ms} = 78\ KHz$$

- **Four operation modes**
  - Standard, edge-aligned PWM
  - Symmetrical, center-aligned PWM for asynchronous motor control
  - Burst-mode for modulated PWM signals
  - Single-shot mode

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PWM unit
Frequencies and Resolution

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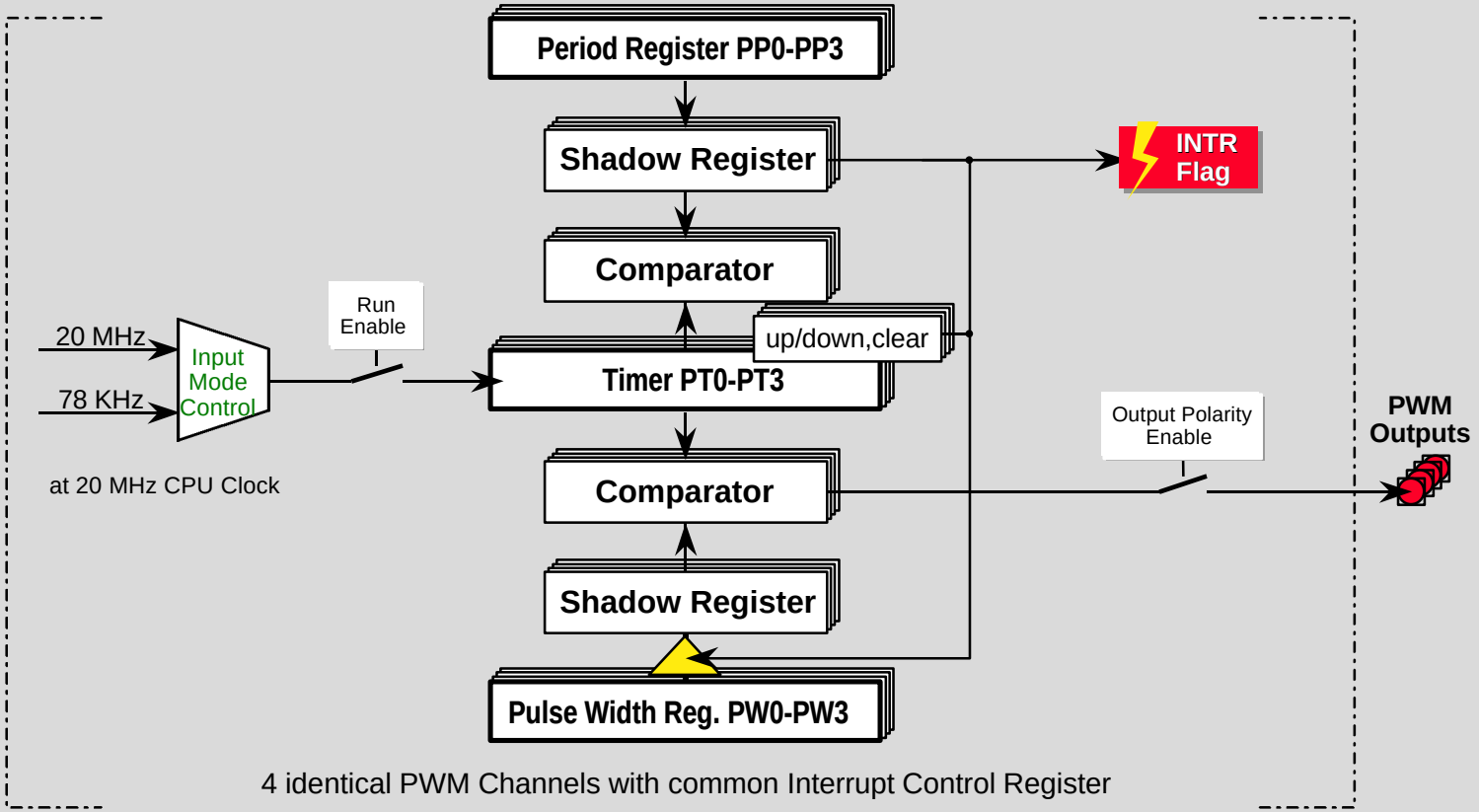
PMW Unit Frequencies and Resolution in Mode 0 Operation (EDGE-ALIGNED)

Resolution → / ↓ Input Clock (CPU @ 20 MHz)	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
CPU Clock (50ns Resolution)	78.1 KHz	19.5 KHz	4.88 KHz	1.22 KHz	305 Hz
CPU Clock / 64 (3.2µs Res.)	1.22 KHz	305 Hz	76.3 Hz	13.1 Hz	4.77 Hz

PMW Unit Frequencies and Resolution in Mode 1 Operation (SYMMETRICAL)

Resolution → / ↓ Input Clock (CPU @ 20 MHz)	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
CPU Clock (50ns Resolution)	39.1 KHz	9.77 KHz	2.44 KHz	610 Hz	152.6 Hz
CPU Clock / 64 (3.2µs Res.)	610 Hz	152.6 Hz	38.15 Hz	9.54 Hz	2.4 Hz

PWM unit
Function Diagramm



4 identical PWM Channels with common Interrupt Control Register

PWM unit
Mode 0 and 1...

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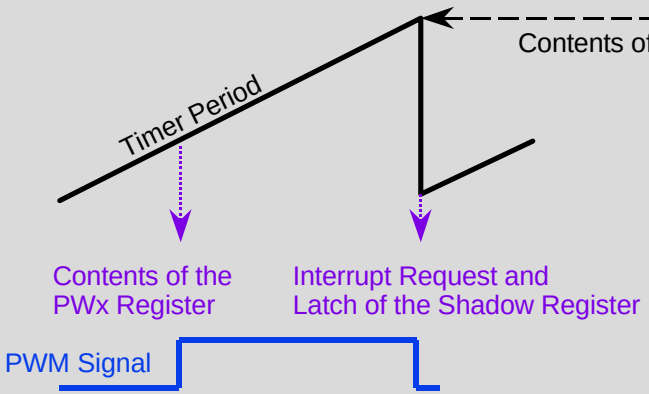
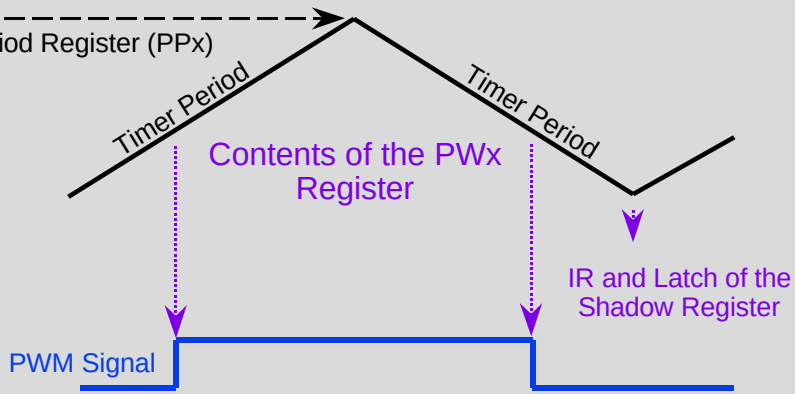
PWM Mode 0:
Standard PWM's or Edge-Aligned PWM's



If all channels are programmed to **mode 0**,
edge-aligned PWM signals will be generated.
A duty cycle from **0 to 100%** is programmable

PWM Mode 1:
Symmetrical or Center-Aligned PWM's

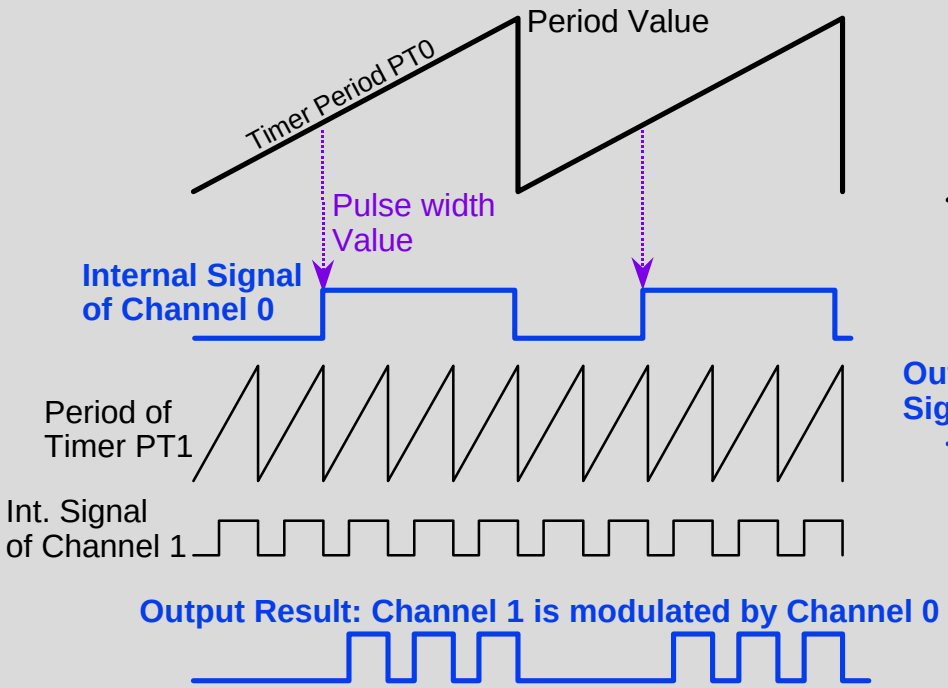


If all channels are programmed to **mode 1**,
center-aligned PWM signals will be generated.
A duty cycle from **0 to 100%** is programmable

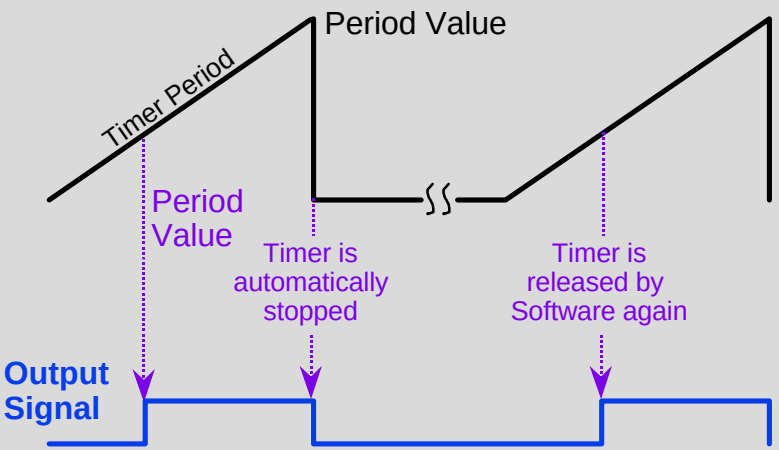
Possible PWM Signals from other channels programmed to the same mode:

... PWM unit
Modes

Burst Mode :
Burst Sequence by combining PWM channel 0 and 1



Single Shot :
Only one PWM Pulse is generated
Mode available for channel 2 and 3



The Timer can be dynamically changed to lengthen (retrigger) or shorten the output pulse

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Analog Digital Converter (ADC)

- **10-Bit ADC based on the successive approximation principle**
  - 9.7µs conversion-time
  - On-chip sample- & hold-circuit (1.6 us sample-time)
  - 16 Multiplexed input channels
  - Automatic self-calibration after conversion
- **Flexible operation mode**
  - Single-channel and single-channel-continuous for periodic data acquisition
  - Auto-scan and auto-scan-continuous for permanent data tracking
  - Channel-injection mode with own result-register can be used to interrupt the scan modes
- **Easy error handling and channel identification**
  - 10-bit result and channel number in result register
  - Overrun error check

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10-Bit A/D Converter Block Diagram

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C164
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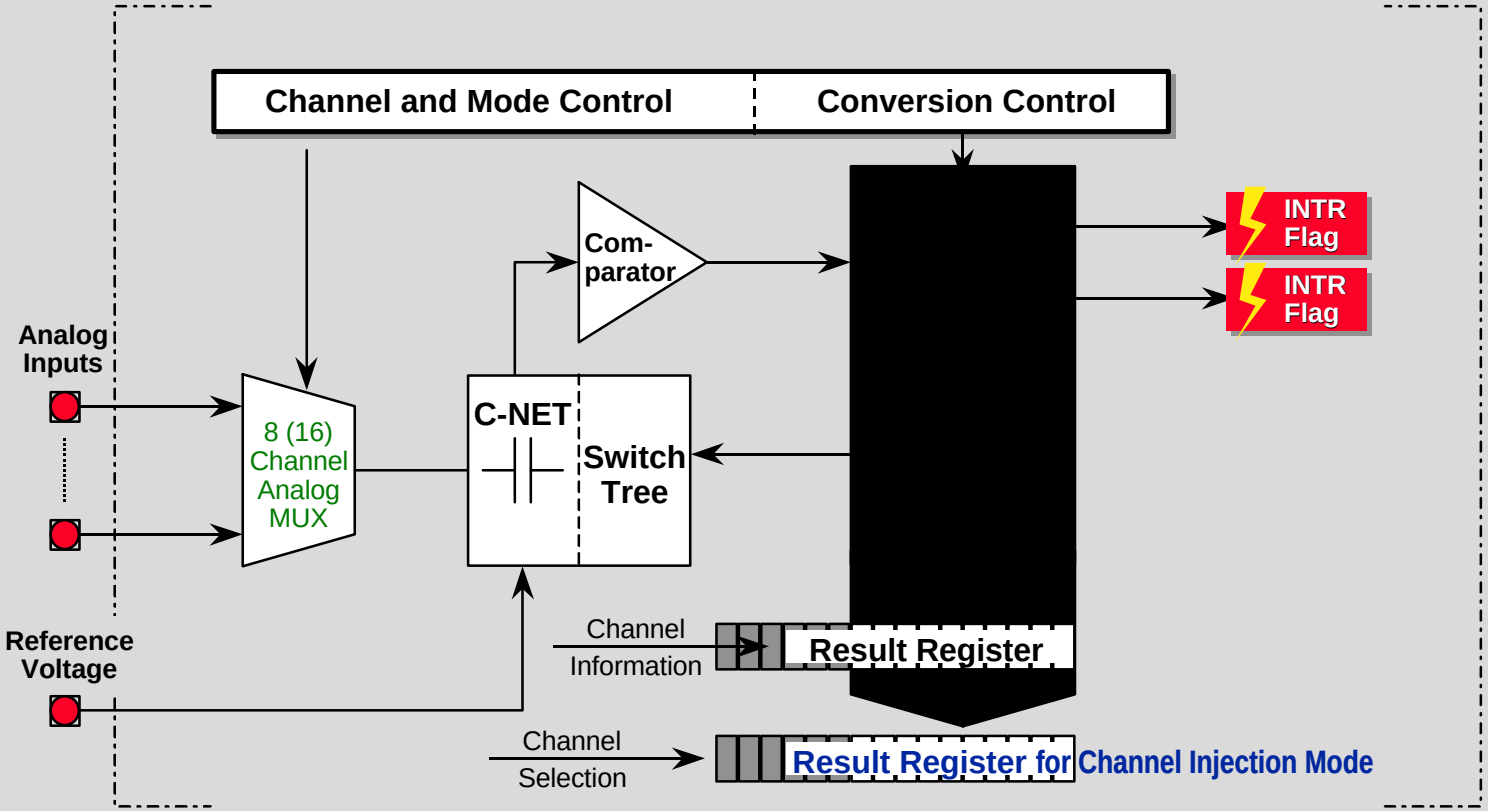

Asynchronous / Synchronous Serial Channel (USART) at 20MHz

- **Synchronous / asynchronous serial channel with its own baud-rate-generator**
- **Asynchronous mode with max 625 KBaud transfer rate**
  - Full duplex (receive and transmit at the same time)
  - programmable features:
  - 1 or 2 stop bits, 7, 8 or 9 data bits
  - Generation of parity- or wake-up bit at data transmission
  - Odd or even parity
  - Error detection (parity, overrun, framing)
  - Wake-up check (receive int. flag is set if wake-up bit is true)
- **Synchronous mode with max 2.5 Mbit/sec transfer range**
  - Half duplex operation (only transmit or receive possible)
  - Easy I/O expansion with external shift register
  - Overrun error detection

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USART
Block Diagram

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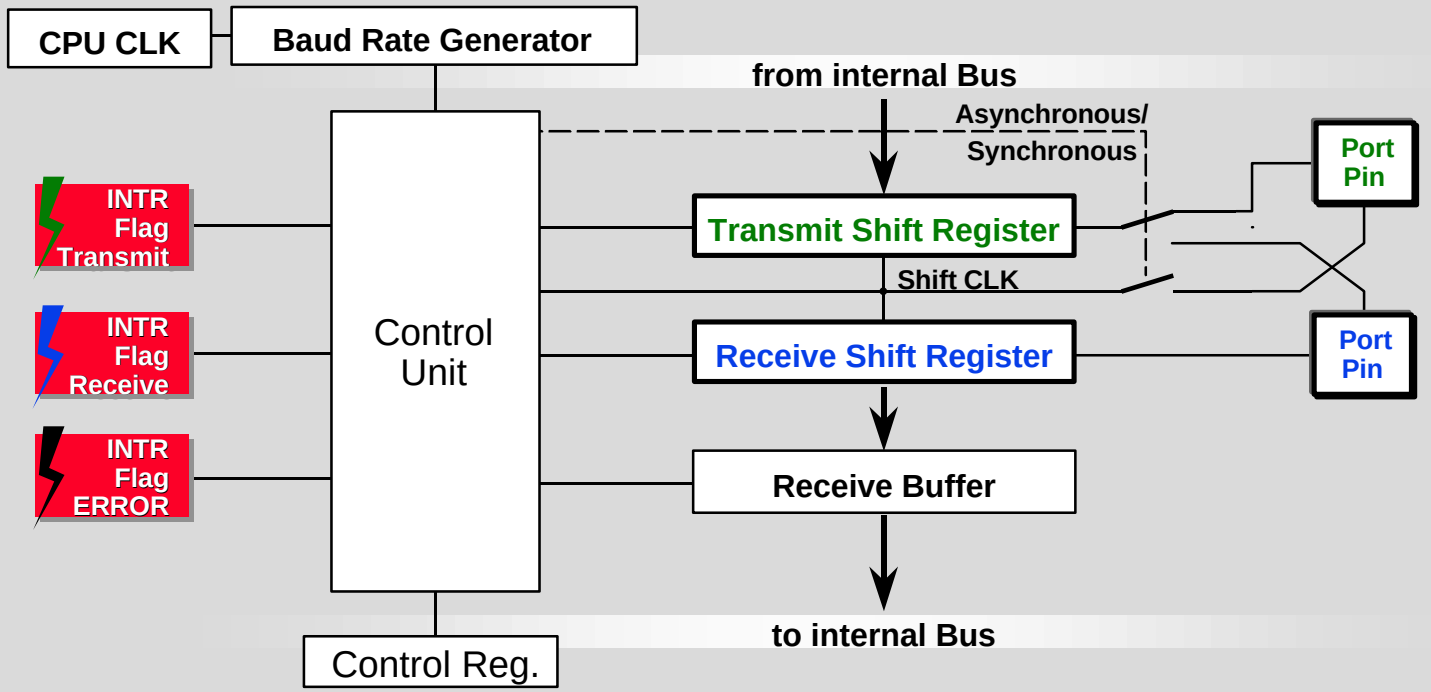
C166
C167

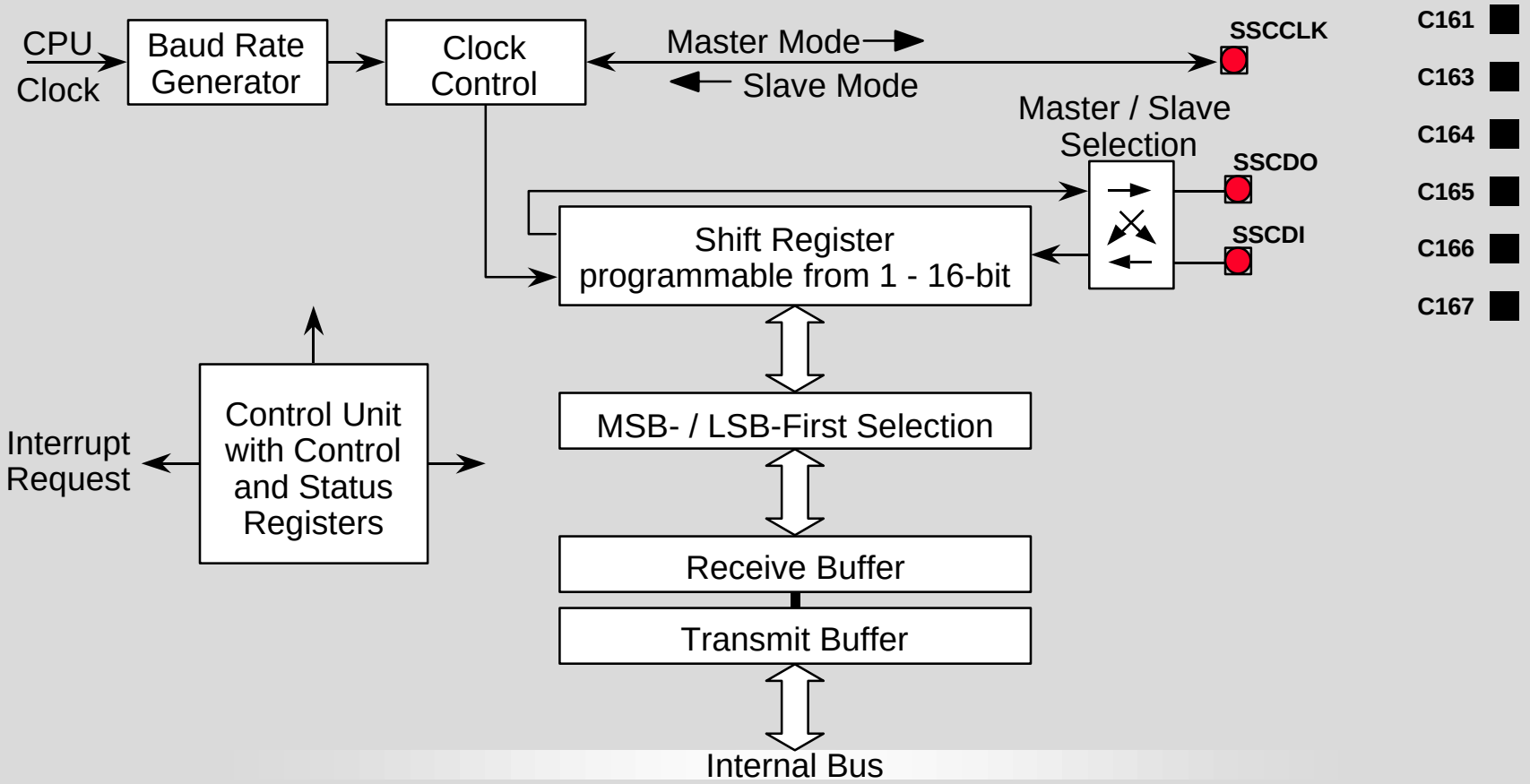


Synchronous Serial Channel (SSC), SPI compatible at 20 MHz

- **Full duplex Synchronous Serial Channel (SSC) with its own baudrate generator for high speed communication**
- **Up to 5 Mbit/sec transfer rate**
- **SPI compatible**
- **Master (clock is output) or slave mode (clock is input)**
- **Programmable features to satisfy various communication requirements**
  - MSB or LSB first
  - Data frame from one to 16-bit
  - Clock polarity and phase

C161	
C163	
C164	■
C165	
C166	■
C167	■

Synchronous Serial Channel - Block Diagram

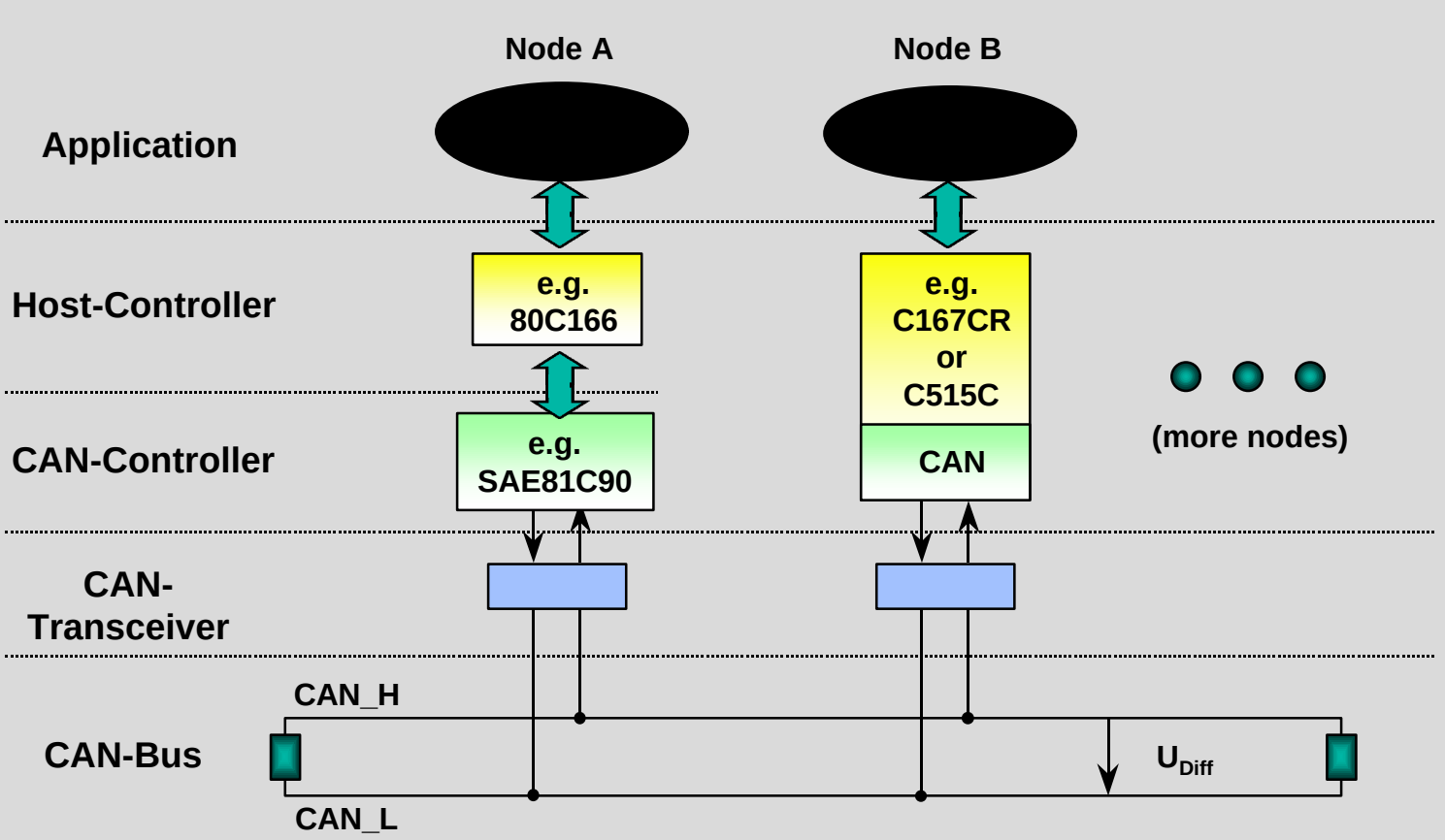


Some things worth knowing about CAN...

- Developed in the mid-eighties by BOSCH
- Asynchronous serial bus with linear bus structure and equal nodes (Multi Master bus)
- CAN does not address nodes (address information is inside the messages combined with message priority)
- Two bus states: dominant and recessive
- Bus logic according to "Wired-AND" mechanism: dominant bits (Zeros) override recessive bits (Ones)
- Bus Access via CSMA/CD with NDA (Carrier Sense Multiple Access/ Collision Detection with Non-Destructive Arbitration)

C161
C163
C164
C165
C166
C167

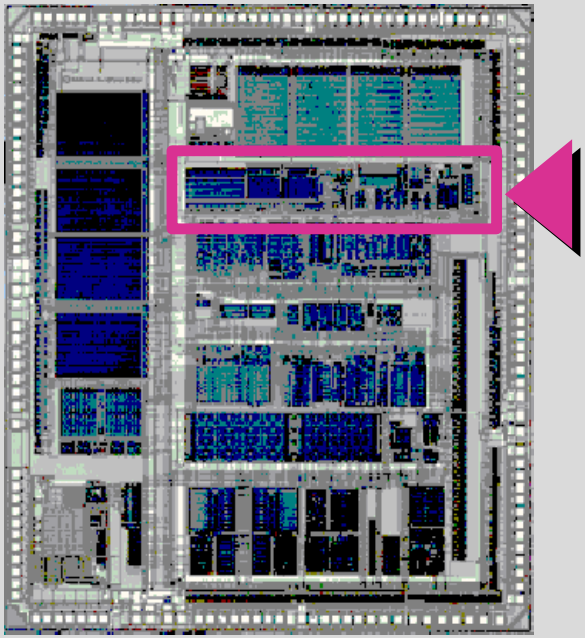
Typical CAN node structure



C161
C163
C164
C165
C166
C167

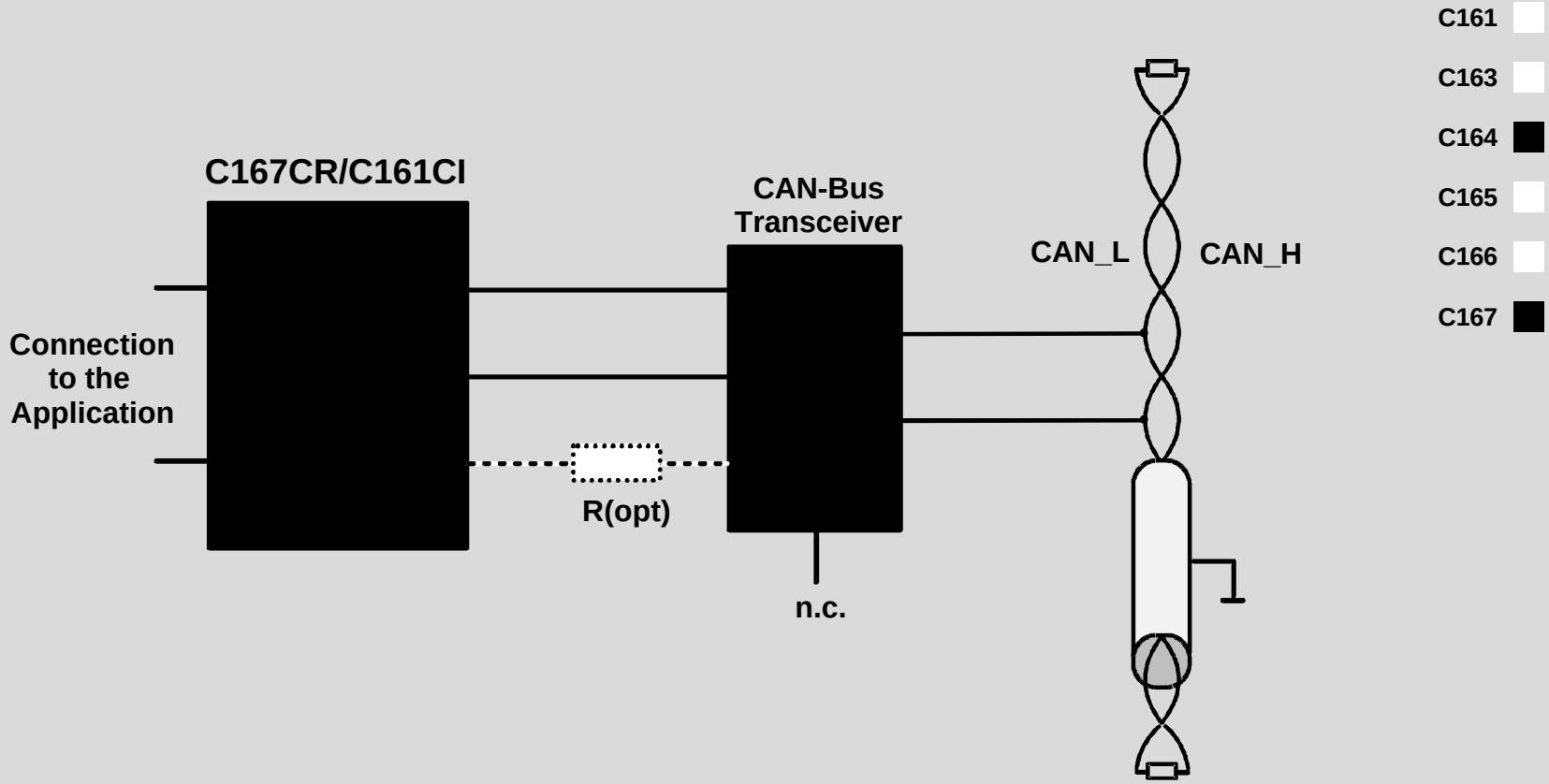
Features of the CAN Module on C167CR / C164CI...

- **Functionality corresponds to AN 82527**
- **Complies with CAN spec V2.0B active (Standard- und Extended-CAN)**
- **Maximum CAN Transfer Rate (1 MBit/s)**
- **Full CAN Device**
  - 15 Message Objects with their own identifier and their own status- and control bits
  - Each Message Object can be defined as Transmit- or Receive Object
- **...**



C161
C163
C164
C165
C166
C167

Connecting the to CAN



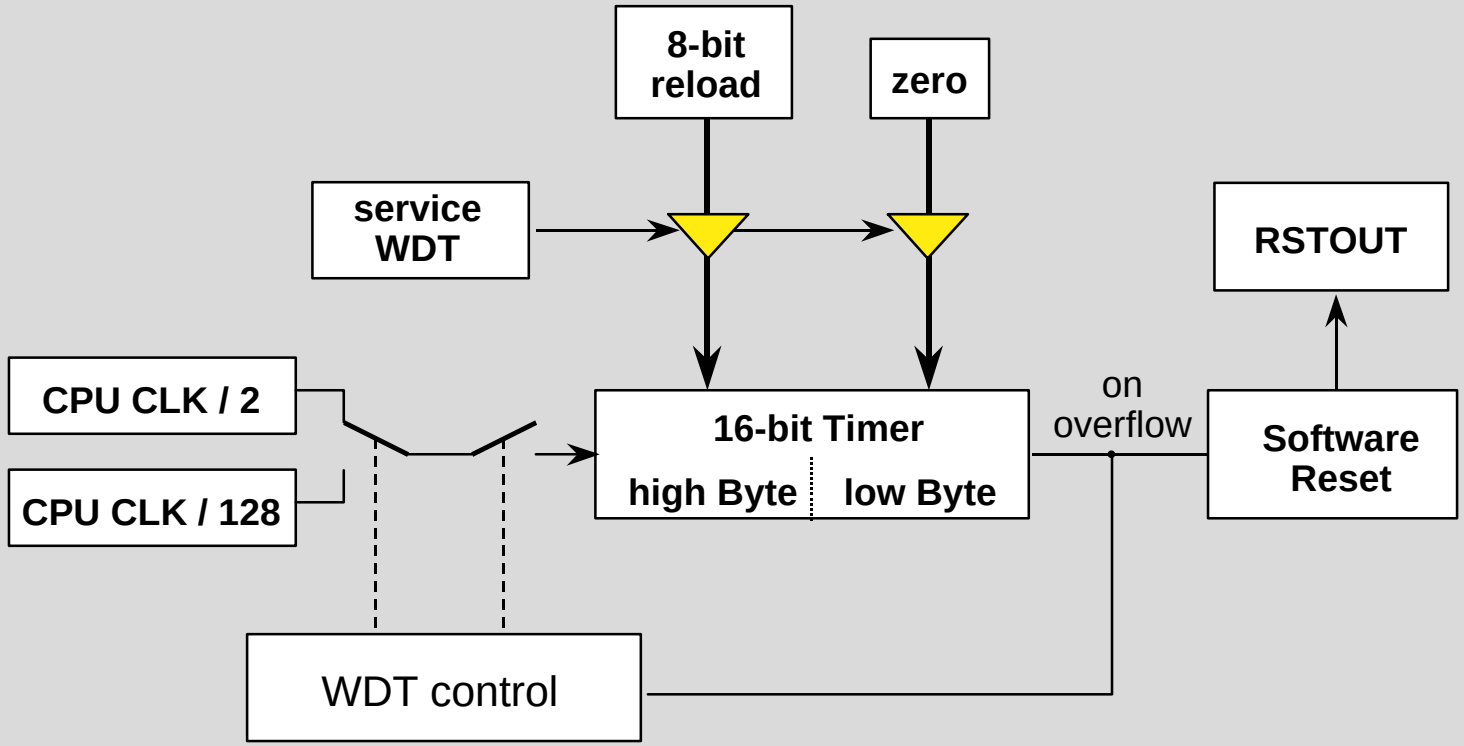
Watchdog Timer (WDT) at 20 MHz

- **16-Bit timer overflow results in:**
  - Software reset
  - Pulls RSTOUT Pin low
  - Sets identification bit and leaves WDT enabled
- **Programmable input clock**
- **High Byte reload register**
- **Timer period from 25.6µs to 470ms**
- **Can be reloaded with a special instruction**

C161
C163
C164
C165
C166
C167

WDT
Block Diagram

C161
C163
C164
C165
C166
C167



Overview Port Structure

- **The Port lines provide the connection to the external world**
  - 77 Port lines on the SAB 80C166
  - 111 Port lines on the C167
  - 77 Port lines on the C165/C163
  - 59 Port lines on the C164
  - 64 Port lines on the C161V/K/O
  - 77 Port lines on the C161RI
- **All Port lines are individually addressable and all I/0 lines are independently programmable for input or output**
- **Each Port line is dedicated to one or more peripheral functions**
- **Each Port is protected with fast diodes**
- **Programmable open drain buffers**
  - P2, 3, 6, 7, 8 on the C167
  - P3, 8 on the C164

C161
C163
C164
C165
C166
C167

Overview Port Structure