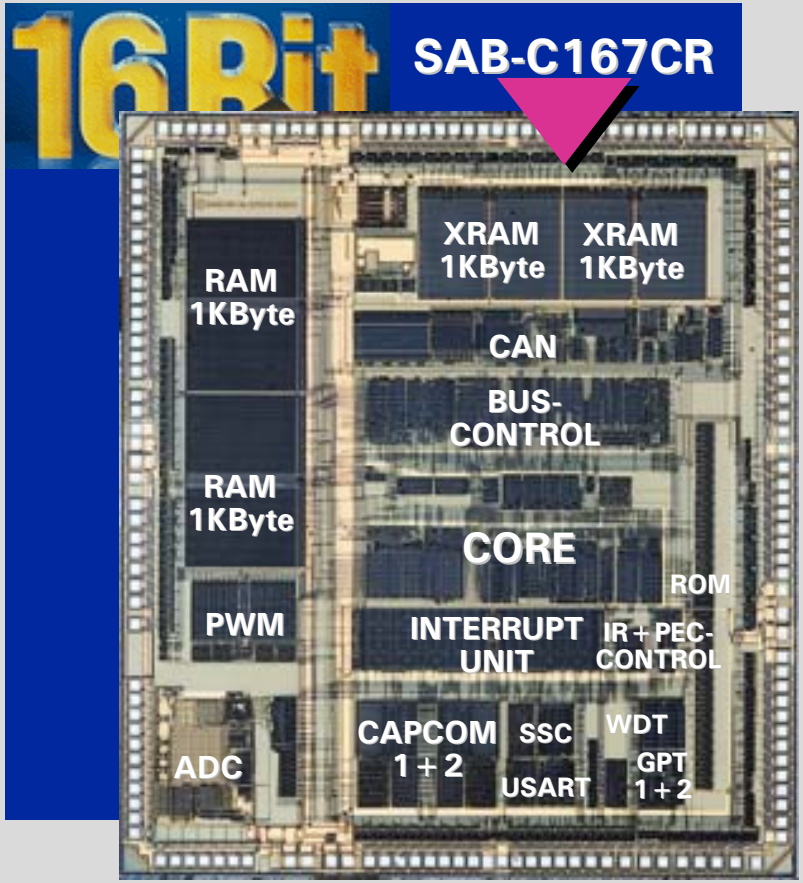
C166 Family-High Performance 16-Bit Microcontrollers



- SAB 8xC166
- C167x
- C165
- C163
- C164x
- C161x

C161
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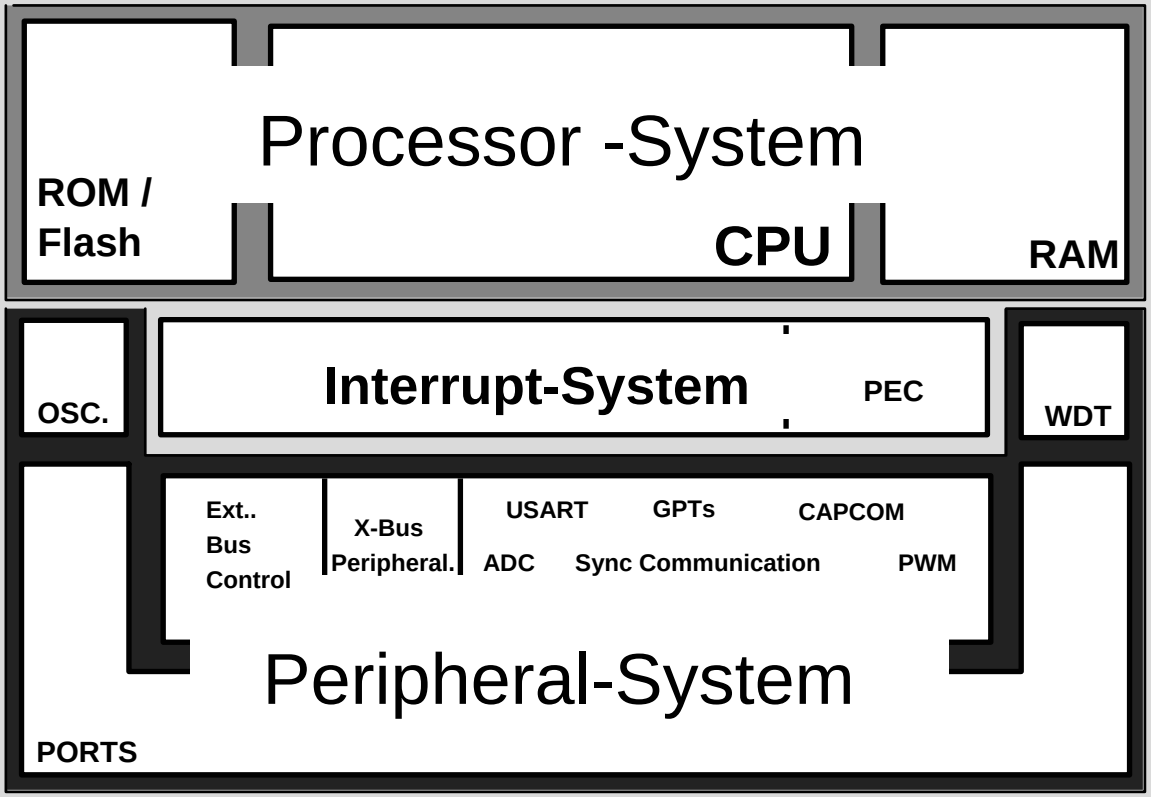
C167

C166 Family
The Three Subsystems

C161
C163
C164
C165
C166
C167



C166 Family
The Best of Both Worlds

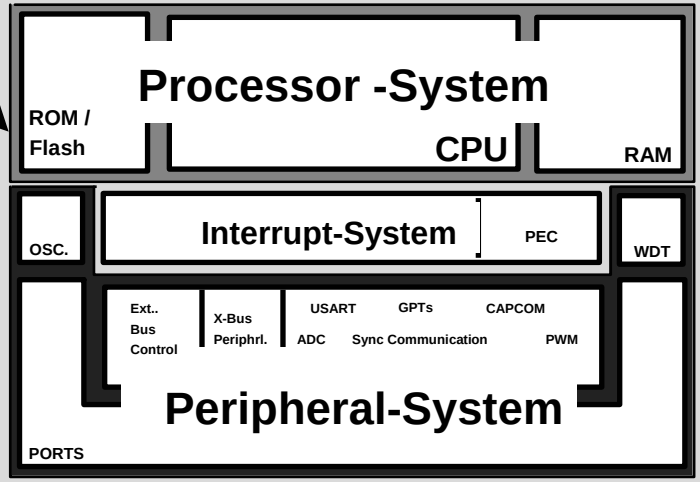
C161
C163
C164
C165
C166
C167

Microcontrollers:

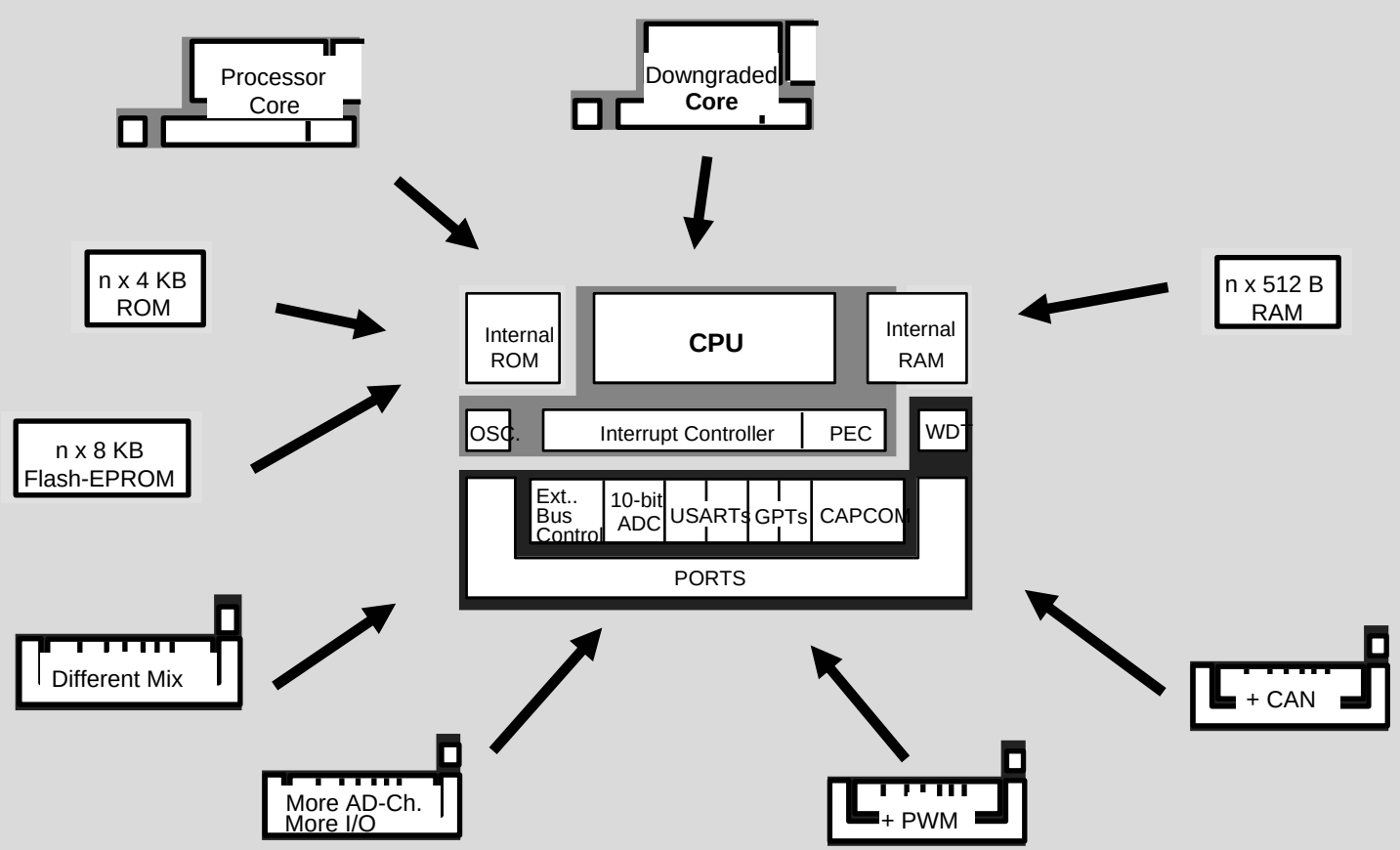
Control oriented instruction set
optimized event handling
"System on Silicon"

Microprocessors:

High computational power
high data throughput
good addressing capabilities
HLL-supporting architecture



The Modular Concept



C161
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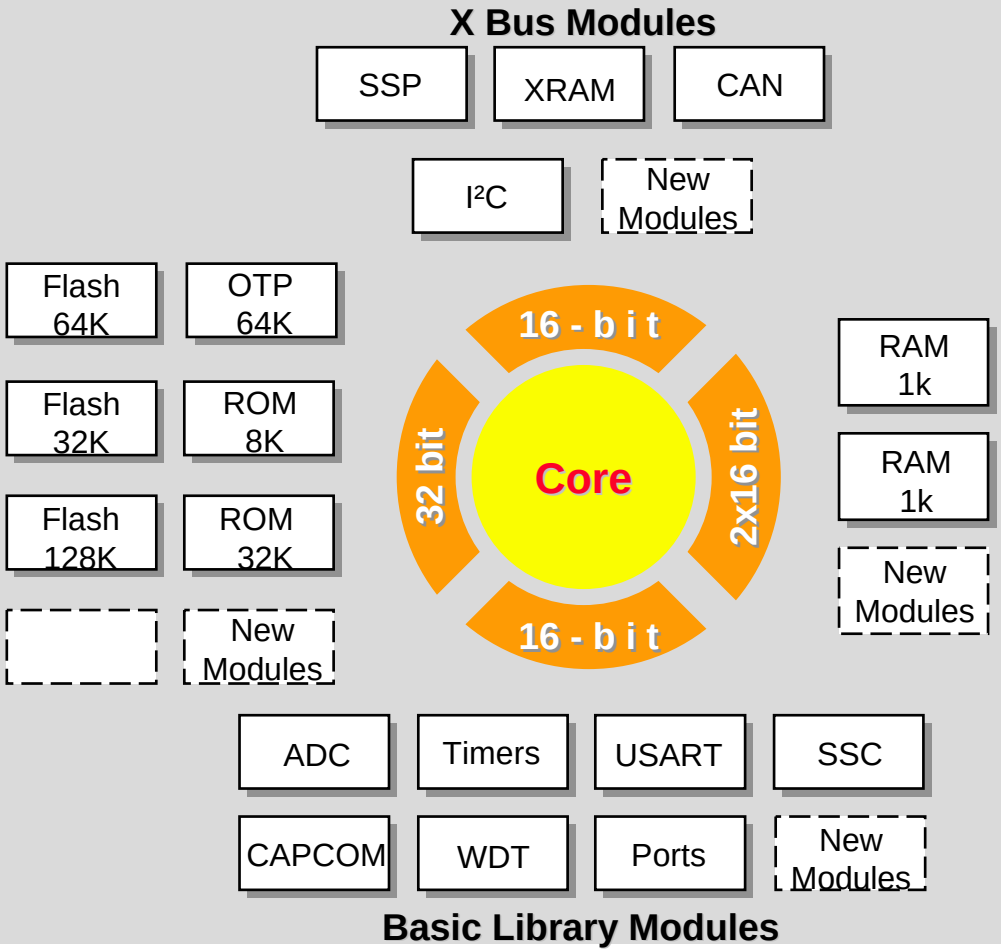
Four Bus Modular System



C161
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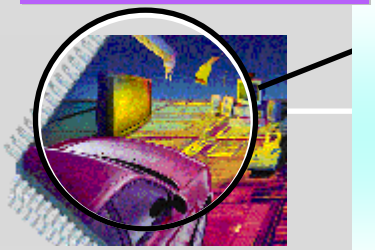
Highly Integrated



* 16 M Address Range
* 2/4 KByte RAM
* 32 CAPCOM
* 4 PWM
* 2 Serial Interface
* 5 Timer
* Chip Selects
  Benefits in System Integration
* Extensive I/O

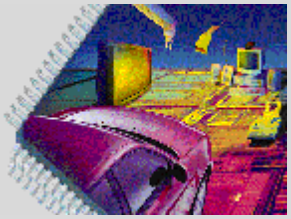
C167
* 2KB RAM

C167S
* 32K ROM
* 2KB RAM
* PLL

C167SR
* 2KB RAM
* PLL

C167CR
* CAN
* 4K RAM
* PLL

General Purpose



Balanced Peripheral set for a broad Application Ranges:
Price differentiation:

* 1K / 2 KB RAM
* ROM / Flash / OTP

* CAPCOM
* PWM
* Serial Interfaces
* Timer
* 10-bit / 8bit ADC
* full Bus Support/ MUX Bus only

8xC166
* 1KB RAM
* 32KB ROM
* 32KB Flash
* P-MQFP-100

C164
* 2KB RAM
* 64KB OTP/ROM/Flash
* Full-CAN 2.0B active
* Power Management / RTC
* CAPCOM6
* P-MQFP-80

Low Cost Processor Oriented

* different RAM Size
* up to 16 M Addr. Range
* up to 5 Timers
* Serial Interfaces SSP, SSC

* less Chip Selects
* full Bus Support/ MUX Bus only
* 3 V Options
* 25 MHz Option

C165
* 2KB RAM
* 3V
* P-TQFP-100

C163
* 1KB RAM
* SSP
* 3V
* reduced Peripherals
* P-TQFP-100

C161x
* 16MHz CPU
* 4 M address
* 1-2KB RAM
* Pwr. Man. / RTC
* P-MQFP-80/100

C161
C163
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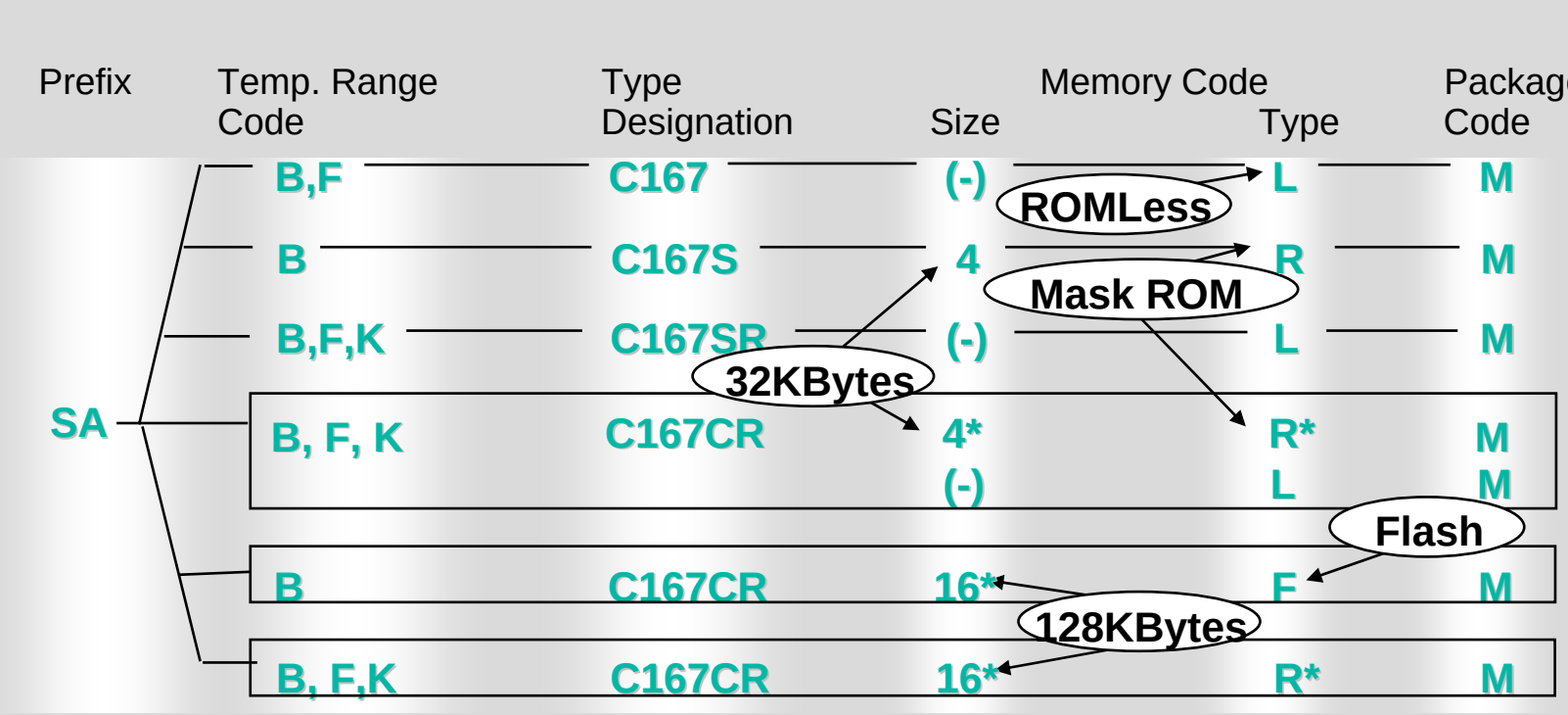
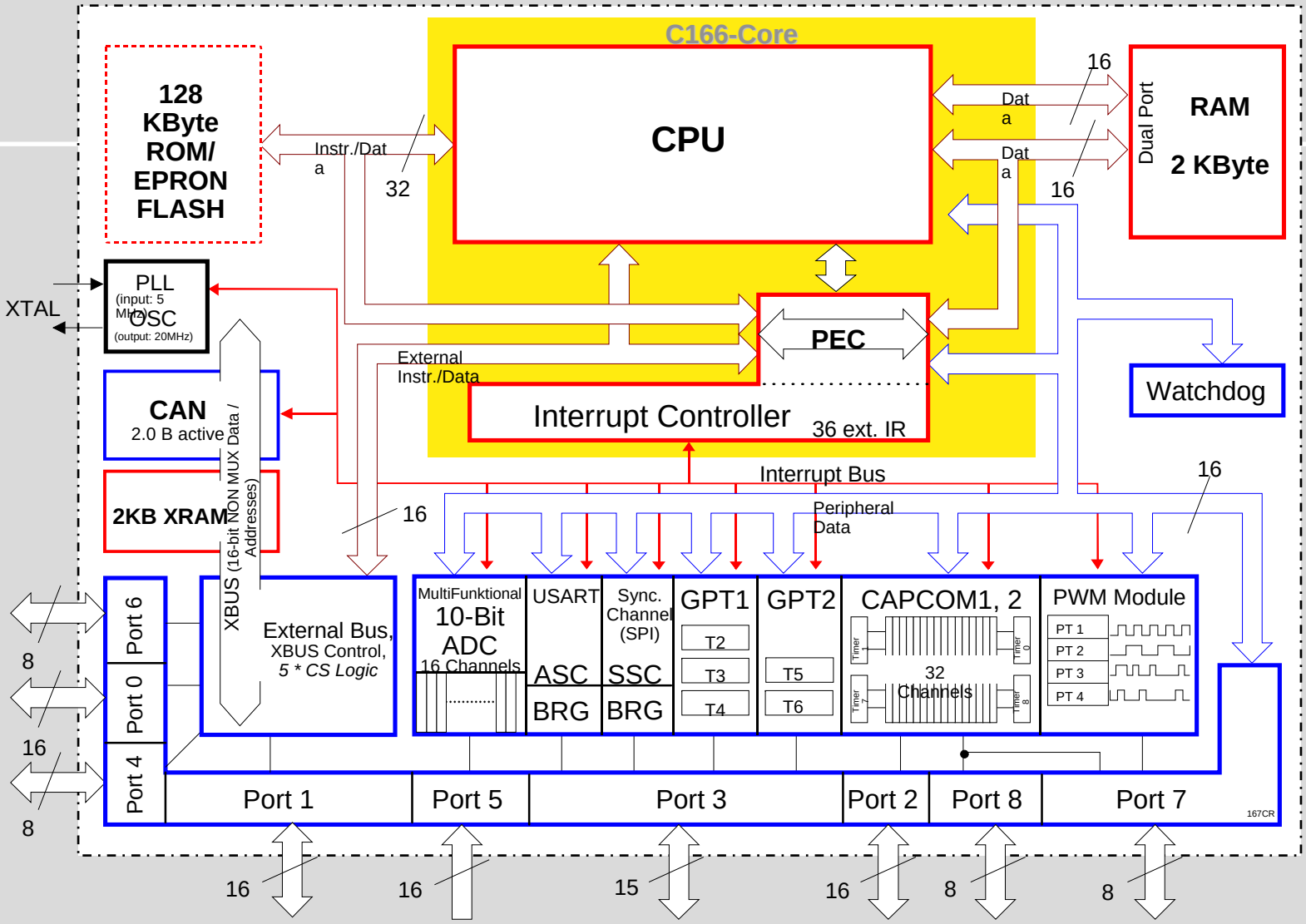
Numbering Scheme
C167 Products



B= 0/ 70 °C
F= -40/ 85 °C
K= -40/110 °C

C= CAN Interface
R= 2KBytes XRAM

M= Metric Quad Flatpack



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Overview - C167CR Block Diagram

Microcontrollers

Overview (20 MHz)

- **Complete 16-bit architecture with 32-bit bus to the internal ROM to process 8-bit, 16-bit and even 32-bit (MUL/DIV) operands**
- **20 MHz CPU clock results in an instruction cycle time of 100ns which guarantees highest CPU performance**
- **To avoid an accumulator bottleneck 16 General Purpose Register (GPR) are implemented**
  - Up to 16 GPRs from a register bank
  - Any register bank is freely locatable in internal RAM
- **Easy and efficient programming is supported by powerful instructions combined with complex addressing modes**
- **Transparent programming of the on-chip peripherals via an universal Special Function Register (SFR) interface**

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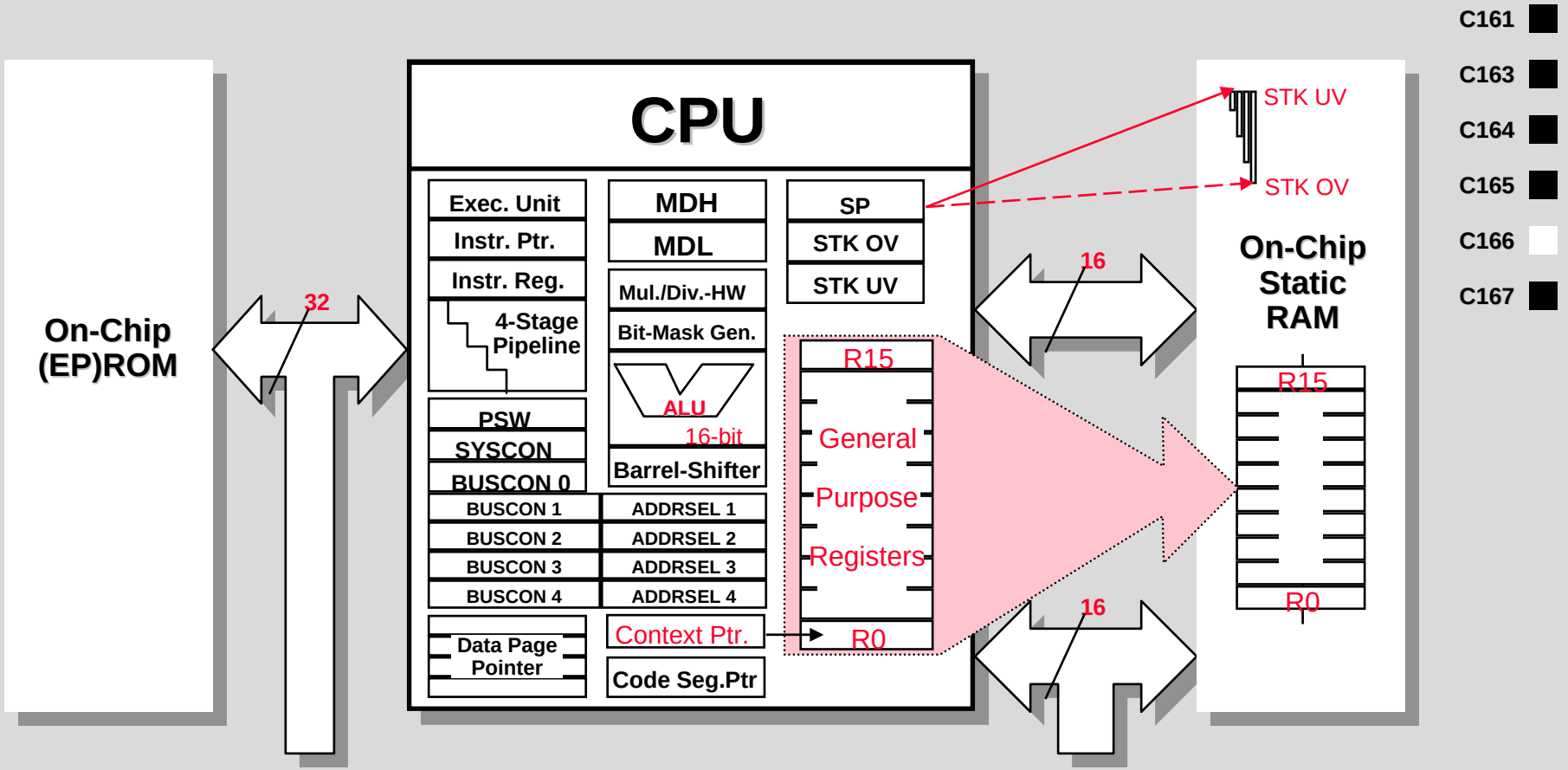
Block Diagram
ROM / RAM interaction

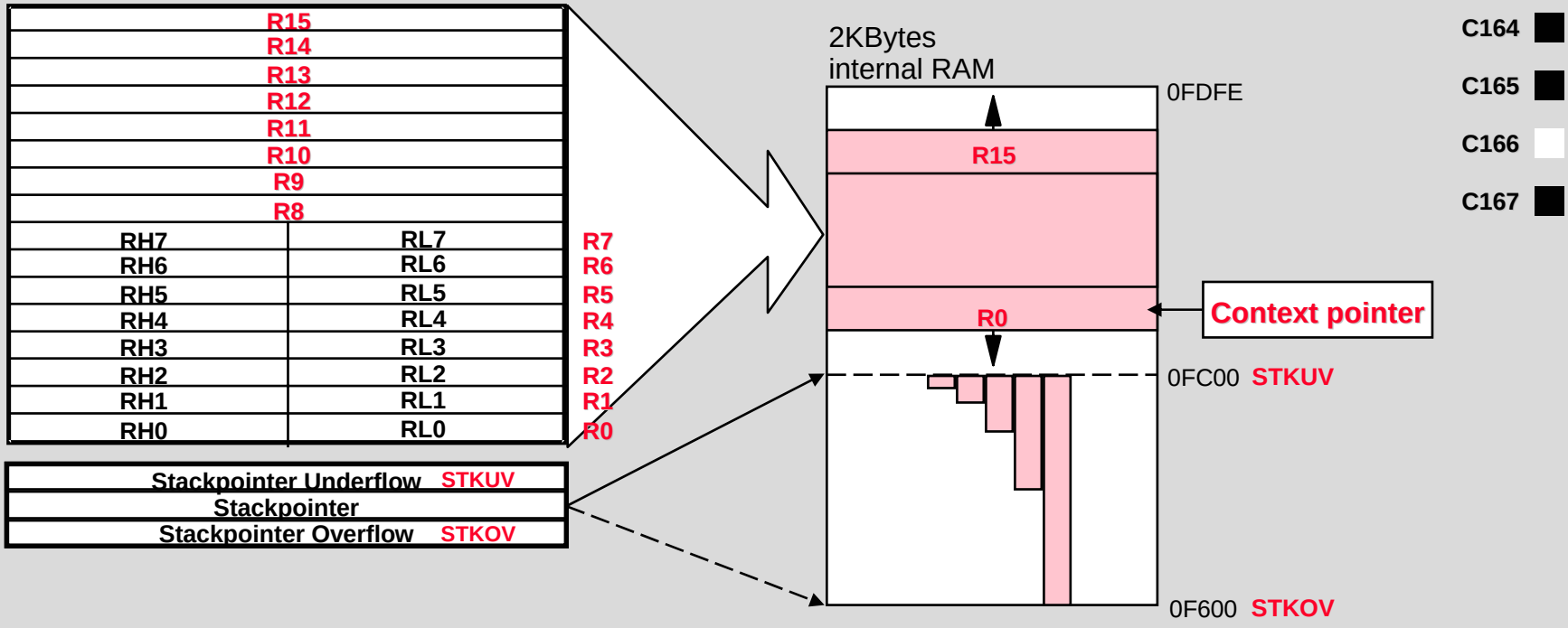


General Purpose Register (GPR)

- **Up to 16 GPRs = 1 Register bank Consisting of max.**
  - 8 Word-Registers
  - 8 Word-Registers with lower and higher Byte access
- **The GPRs are bit-addressable**
- **Any Register bank can be freely allocated in internal RAM**
- **The location of the active Register bank is determined by Context Pointer (CP)**
- **CP can be easily switched, to select another Register bank**
- **SWTC (one instruction cycle)**

C161 ■
C163 ■
C164 ■
C165 ■
C166 ■
C167 ■

Block Diagram
ROM / RAM interaction with 2K RAM



Four Stage Instruction Pipeline at 20 MHz

- **Effective execution time of most instruction in 100 ns**
- **Three word prefetch queue (buscontroller) to support pipeline**
- **Optimized branch processing**
  - For branch instruction (Jump, Cond. Jump, Call, Return,...) only one additional machine cycle is normally required to fetch target instruction
- **Jump Cache**
  - For loop processing no additional machine cycle is required

C161
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Four Stage Instruction Pipeline at 20 MHz

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C166
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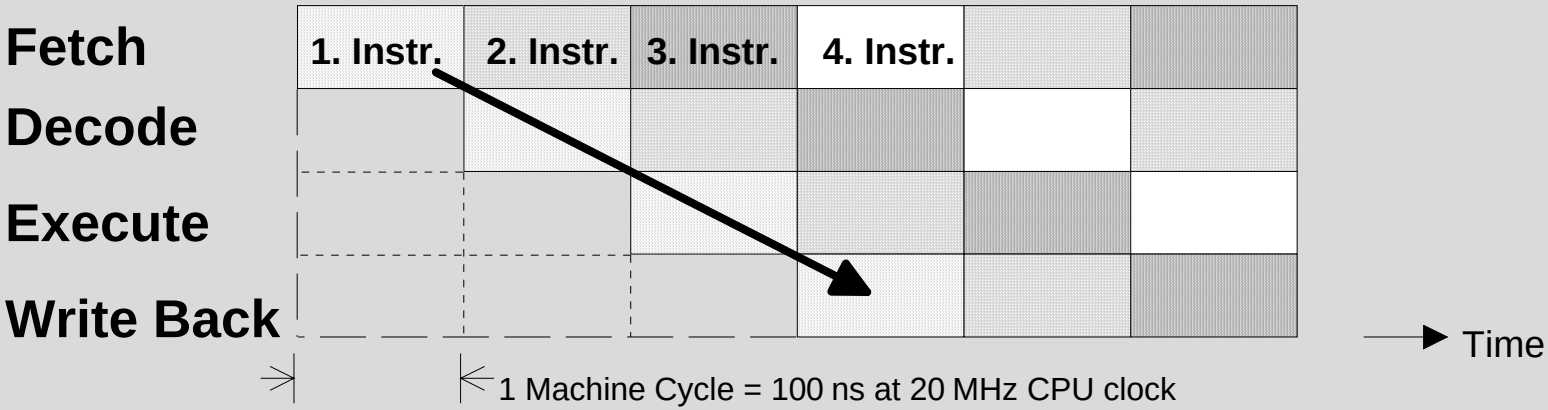
Processing of each instruction is partitioned in 4 stages



Instruction Set at 20 MHz

- **Data manipulation**
  - Arithmetic and boolean instruction incl. fast multiply/divide in 0.5/1.0us
  - Multiple (up to 15) bit shift and rotate in 100 ns
  - Bit to bit manipulation in internal RAM and SFR's
- **Data movement**
  - MOV instructions with all important addressing modes
  - Byte to word conversion
  - System stack (PUSH, POP) with over- and underflow control
  - User stack (MOV with auto increment and decrement)
- **...**

C161
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...Instruction Set at 20 MHz

- **Program manipulation**
  - Jumps and calls / conditional jumps under 16 different conditions
  - Software- and hardware-Traps
  - Fast context switching in 100 ns

- **Special instructions for**
  - Power consumption reduction and system Control
  - Non-interruptable instruction sequences
  - Extended addressing access

C161
C163
C164 ■
C165
C166
C167 ■

Address Space...

- **Complete address space**
  - "von Neumann" architecture with multiple internal bus structure to avoid bus bottlenecks
  - 64KByte non-segmented address space
  - up to 16 MBytes
  - segmented address space: 64KB code segments and 16K data pages

- **Internal address space**
  - up to 128 KBytes ROM / Flash-EPROM
  - max 4 KByte SFR's

	C167	C167CR
RAM	4 KByte	4 KByte
ROM	128 KByte Flash	128 KByte Flash

C161
C163
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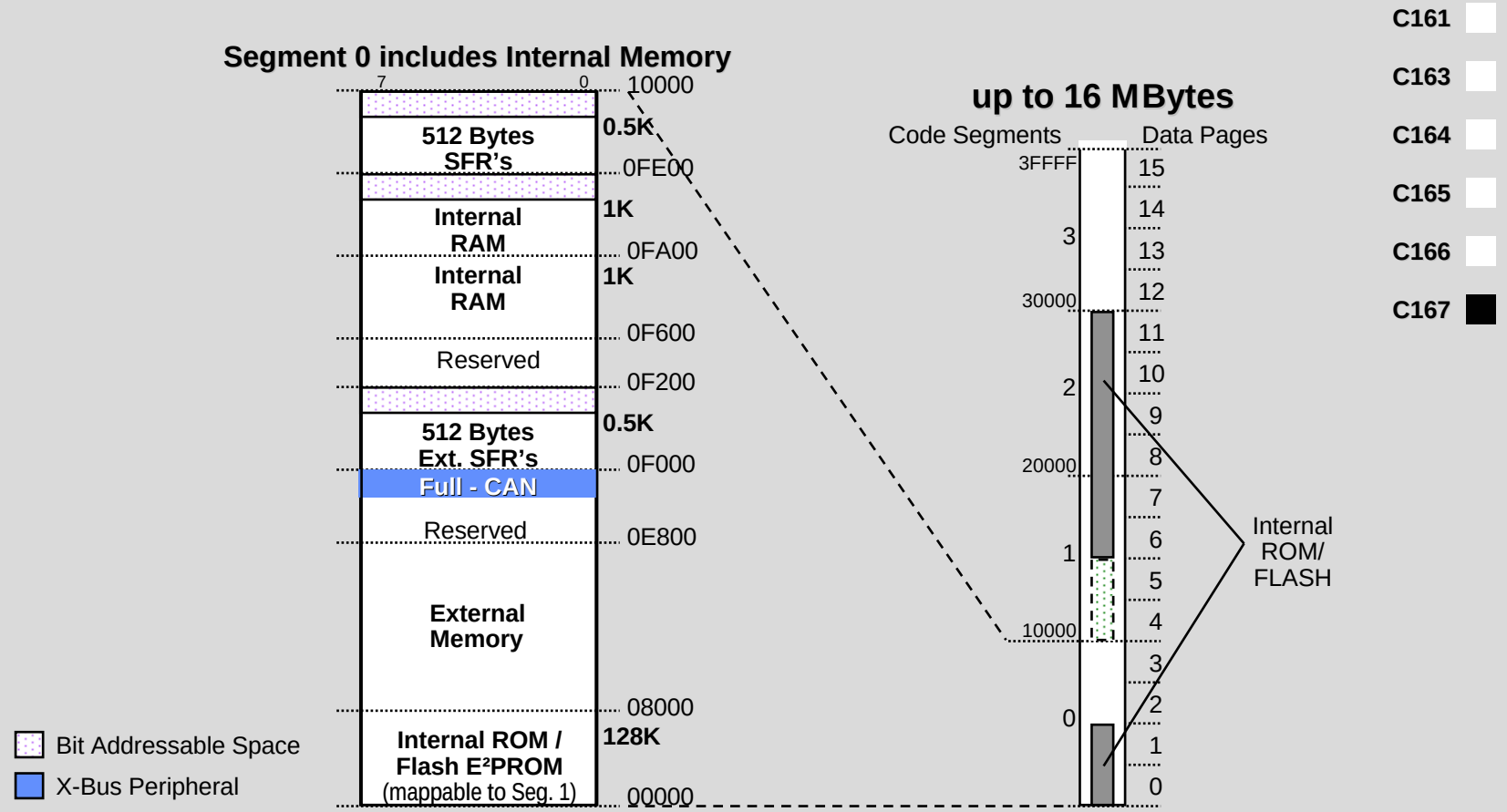
C165
C166
C167

...Address Space

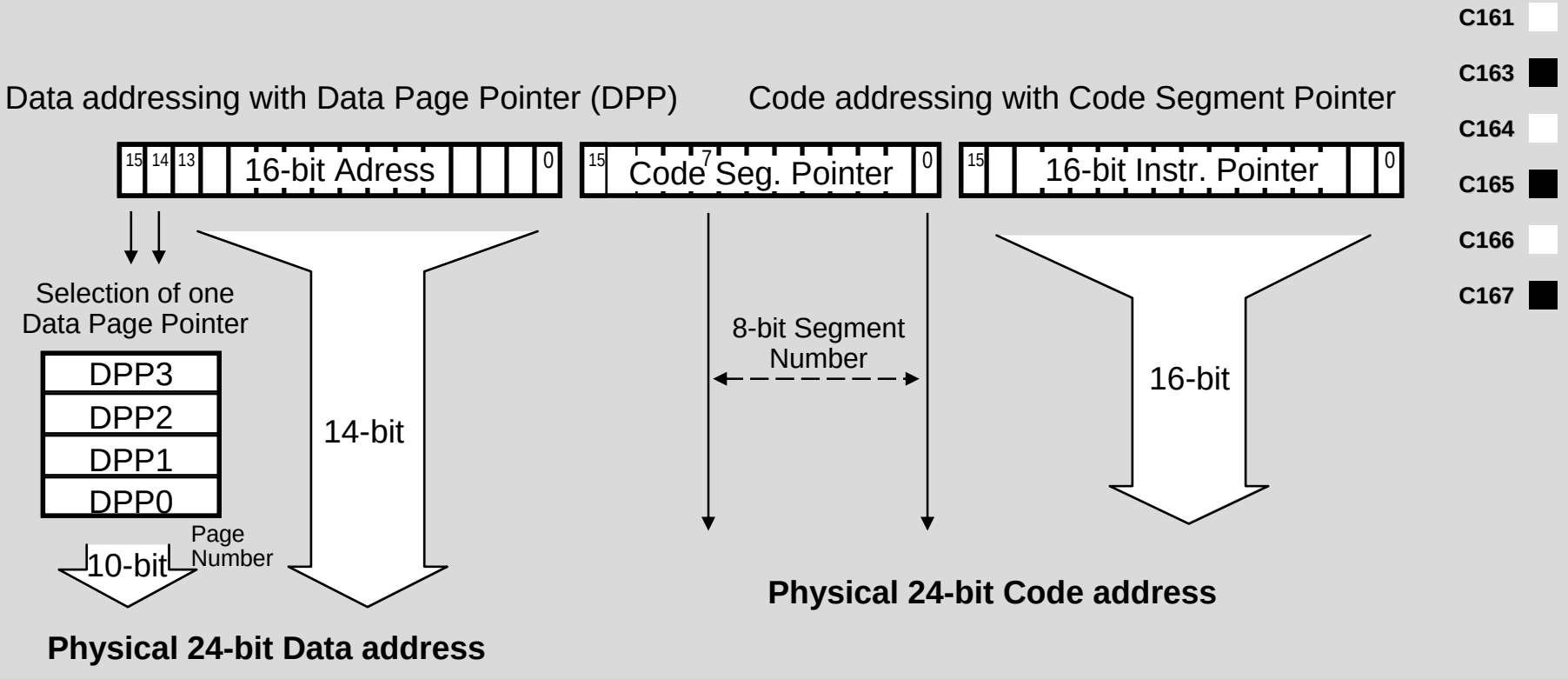
- **Flexible ext. bus configurations to simplify system integration**
  - up to 24-bit Address / 8-bit Data (MUX and NMUX)
  - up to 24-bit Address / 16-bit Data (MUX and NMUX)
  - Five completely independent configuration registers
  - Five programmable chip selects and programmable bus control signal to save external glue-logic
  - Programmable HOLD/HOLDA/BREQ bus arbitration function for multi-master operations

C161 ☐
C163 ■
C164 ☐
C165 ■
C166 ☐
C167 ■

Internal and external Memory Map - C167CR



Code and Data Addressing via Segmentation and Paging on 16 Mbyte address range



Data Addressing via Data Page Pointer (DPPx)

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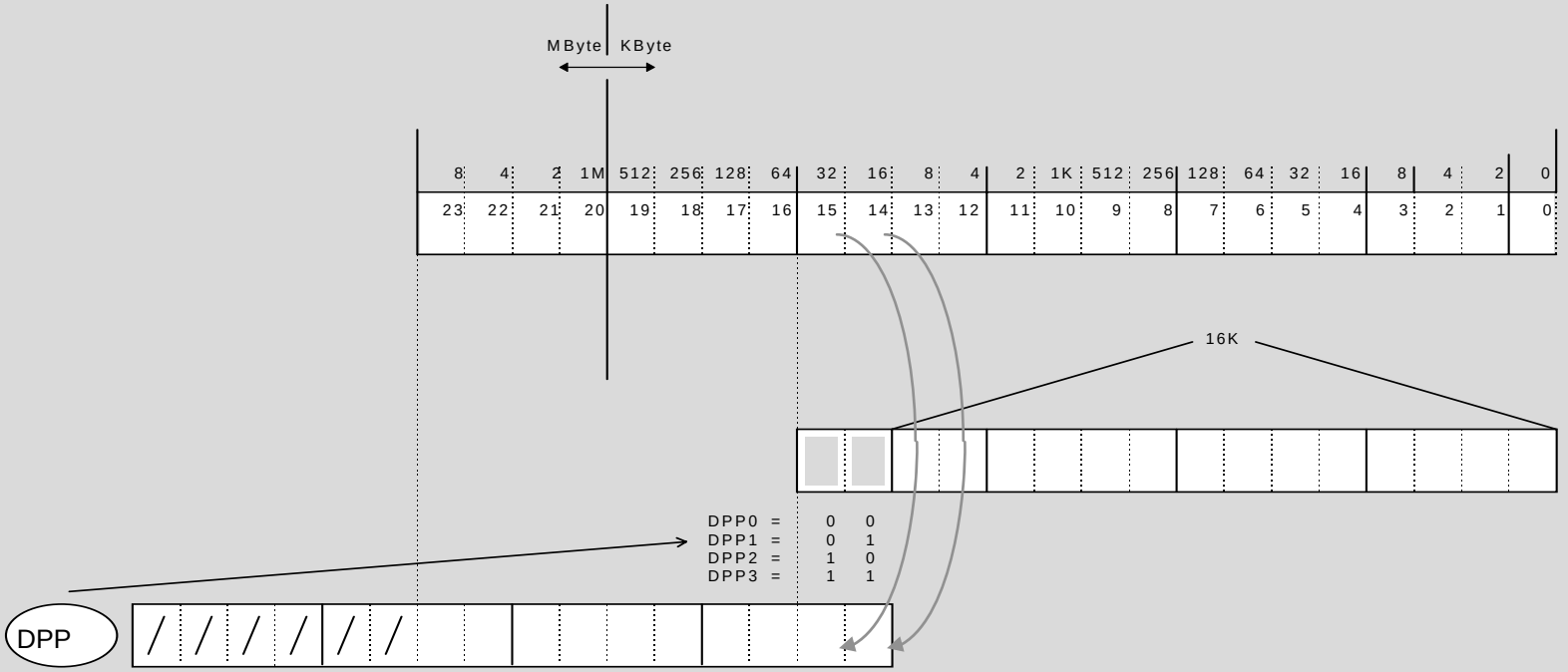


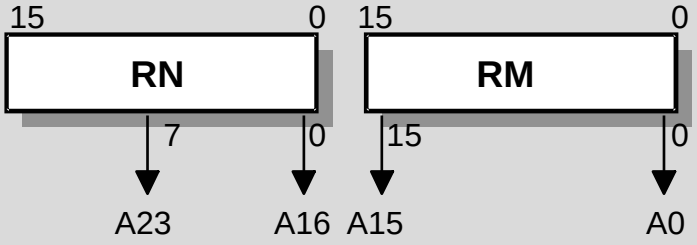
Data Addressing via Extended Mode

- **Overrides standard DPP addressing scheme to ease large (up to 32-bit) address calculation**
  - Segment or Page override by an immediate value
  - Segment and Page override by a Register contents

C161 ■
C163 ■
C164 ■
C165 ■
C166 □
C167 ■

Examples: **Override Segment Number**

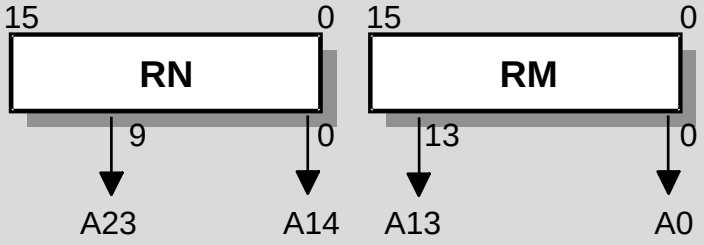
```
EXTS RN,#data2 ;data2:No. of instructions
MOV [RM],Ri    ;to be used for Ext.Addr.Mode
```



Physical address, where the contents of Ri is moved to

Override Page Number

```
EXTP RN, #data2
MOV [RM], Ri
```



Physical address, where the contents of Ri is moved to

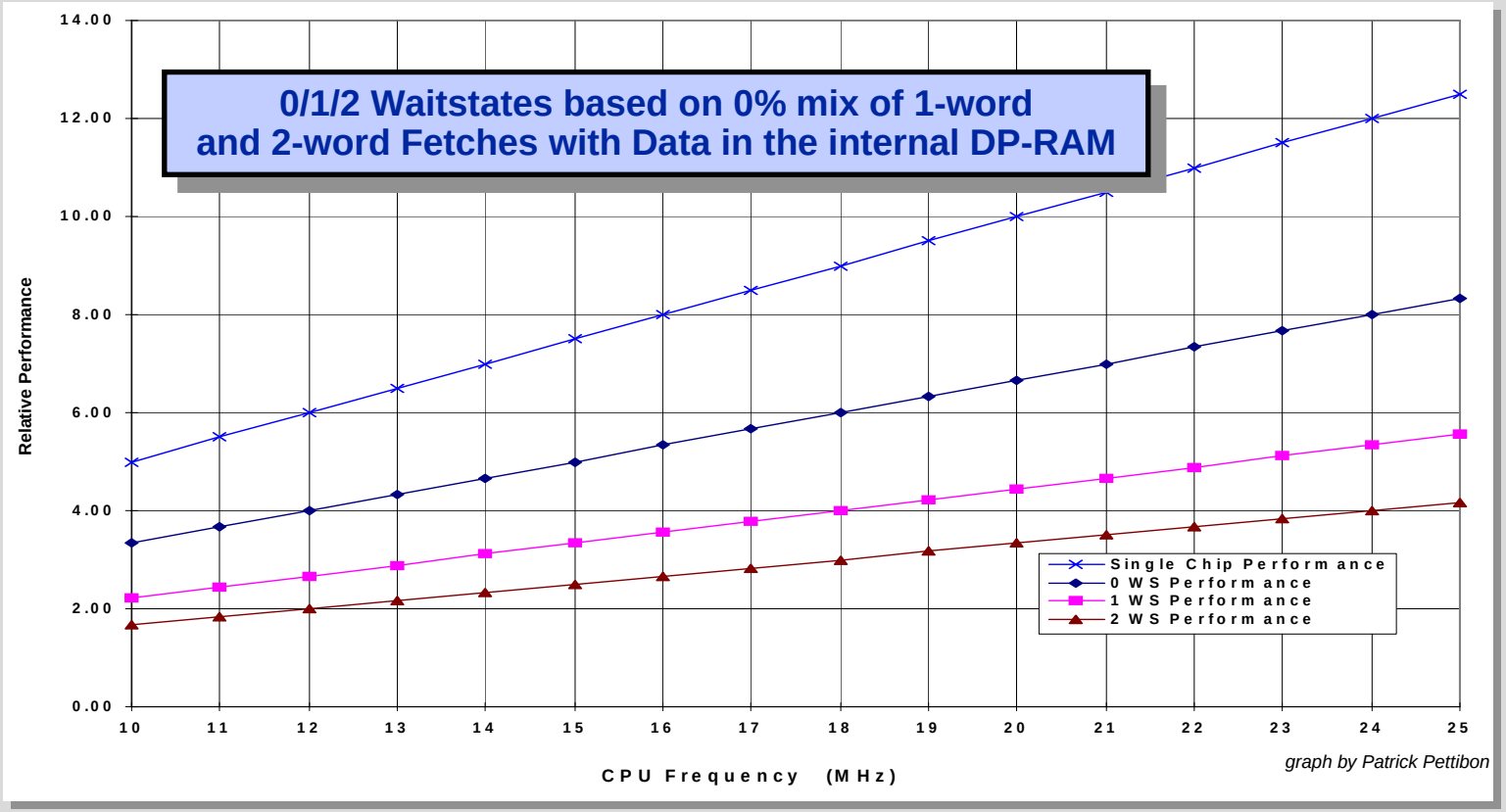
Comparison of Bus Speed at Different Bus Configurations at 20 MHz CPU Clock

C161 □
C163 □
C164 ■
C165 □
C166 ■
C167 ■

	single Chip Mode	16 Bit Data 16/24 bit Address NON MUX	16 Bit Data 16/24 bit Address MUX	8 Bit Data 16/24 bit Address NON MUX	8 Bit Data 16/24 bit Address MUX
used Ports	none	Port 0, 1, 4	Port 1, 4	Port 0, 1, 4	Port 1, 4
Address Latch	none	none	16 Bit	none	8 Bit
Bus Cycle Time 0 / 1 / 2 Wait States	100ns /../..	100/150/200 ns	150/200/250 ns	100/150/200 ns	150/200/250 ns
Instr. Fetch Time 1 Word	100ns /../..	100/50/200 ns	150/200/250 ns	200/300/400 ns	300/400/500 ns
Instr. Fetch Time 2 Word	100ns /../..	200/300/400 ns	300/400/500 ns	400/600/800 ns	600/800ns/1µs
EPROM Access Time t17	n.a.	70/120/170 ns	70/120/170 ns	70/120/170 ns	70/120/170 ns
rel. speed for typ. code (50% 2 word instructions)	1	1.5	2.5	3.0	4.5

☞ **External bus speed optimization by prefetching into the instruction queue !**

Relative Performance vs. CPU Frequency



C163 Flash
Comparsion with C167CR Flash

C163 Flash Module
New Technology

128 KByte capacity
Any use for instruction code or data

Programming and erase
+ Progr. voltage 5V on standard VCC pins
+ Integrated state machine
+ Directly controlled by commands

Programming control
+ Fast: 125 msec per 8 KB block

Erase control
+ Simple erase command per sector
+ Fast: 10 msec per sector

C167 Flash Module

128 KByte capacity
Any use for instruction code or data

Programming and erase
- 12 V on separate VPP pin
- SW controlled
- Complex SW to avoid over/under-programming or erase

Programming control
+ Fast: 200 msec per 8 KB block

Erase control
- Preprogramming (all zeros) necessary
- Slow: 1 sec per sector

Overview at 20MHz...

- **Interrupt Controller**
  - Extremely short interrupt response time of minimal 250ns typical: 400ns
  - Interrupt execution in small time segments
  - Ensures highest real-time performance
  - Comprehensive prioritization scheme
    - **Easy scheduling of complex real-time systems by using up to 64 priority levels (4 groups within 16 levels)**
  - Non-maskable interrupt input (NMI)
  - Hardware-Traps on runtime errors and Software-Traps
- **...**

C161
C163
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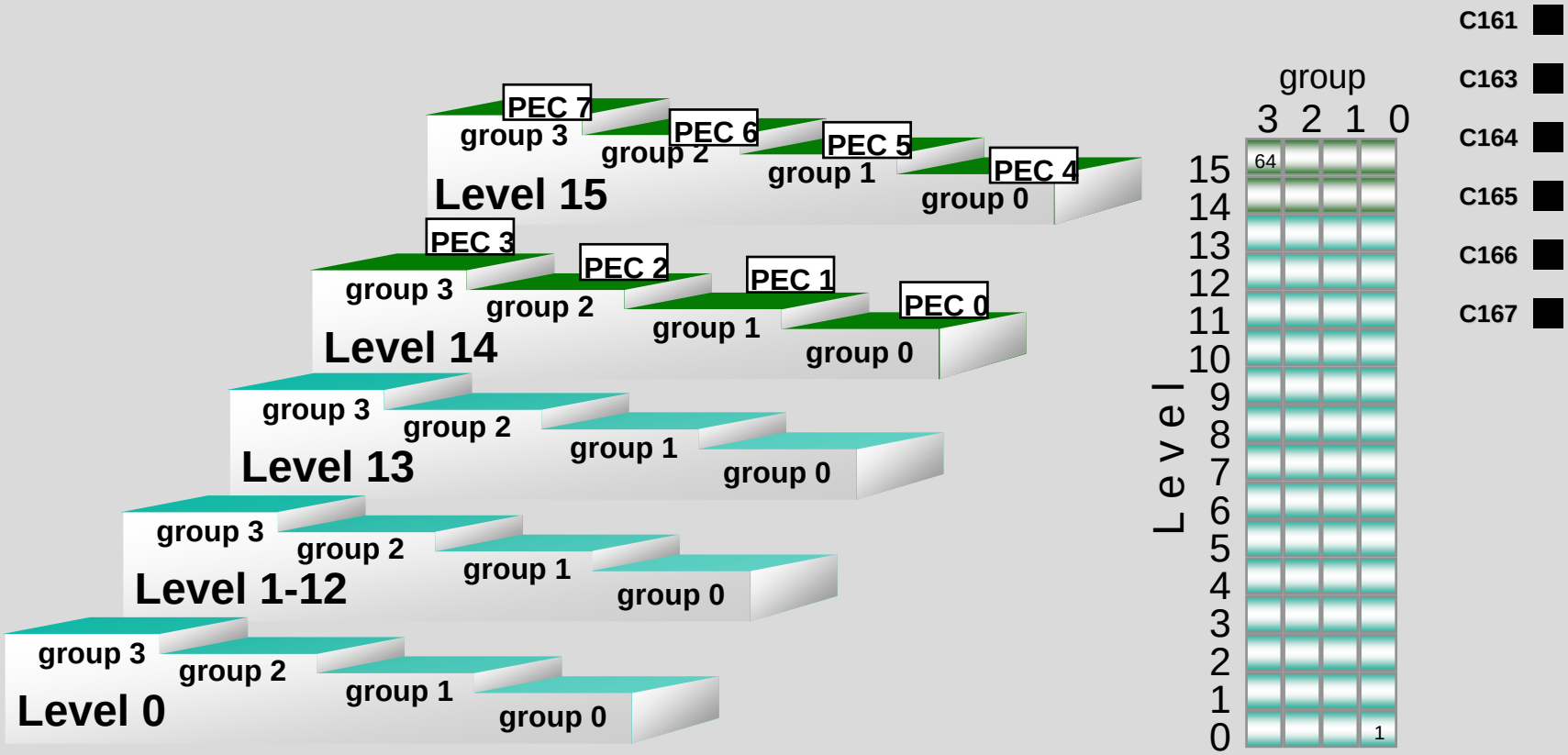
...Overview at 20MHz

- **CPU independent interrupt-service via Peripheral Events Controller (PEC)**
  - Off-loads the CPU from simple but frequent interrupt-services
  - Interrupt-driven “DMA-like” data transfer to any location in segment 0, without task switch of the CPU
  - Makes peripheral data transfers Independent of running CPU routine
  - Response-time is minimal 150ns, typical 300ns with a CPU load of 100ns

C161 □
C163 □
C164 ■
C165 □
C166 ■
C167 ■

Priority System, PEC



Interrupt Processing

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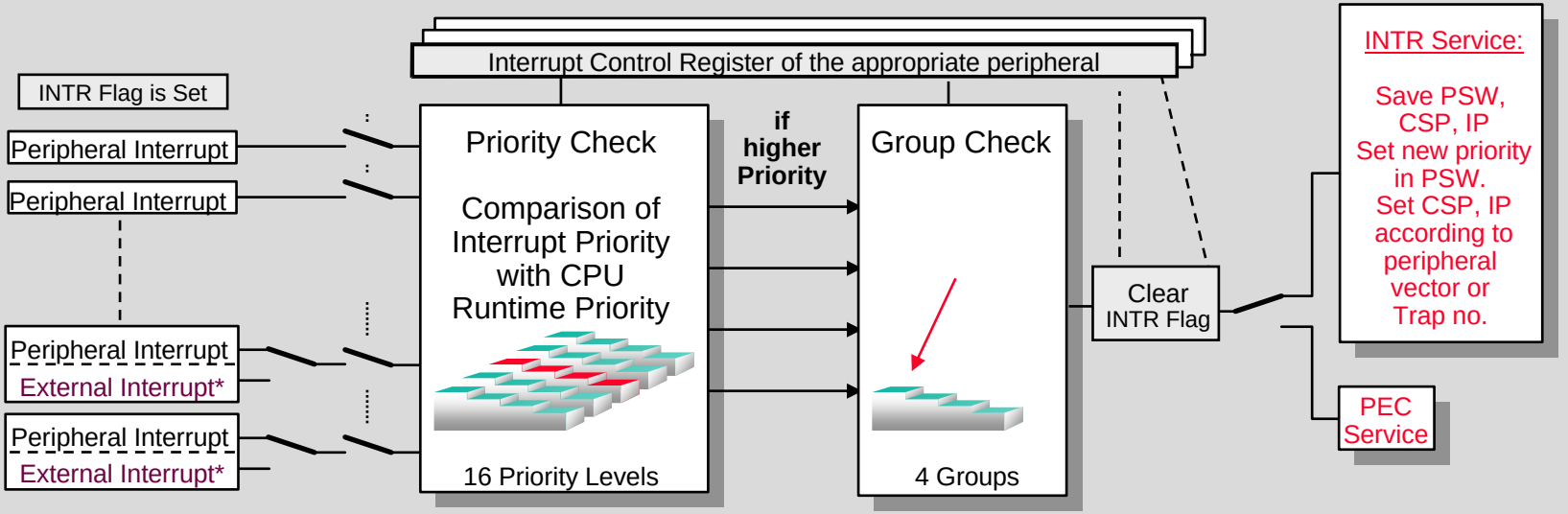
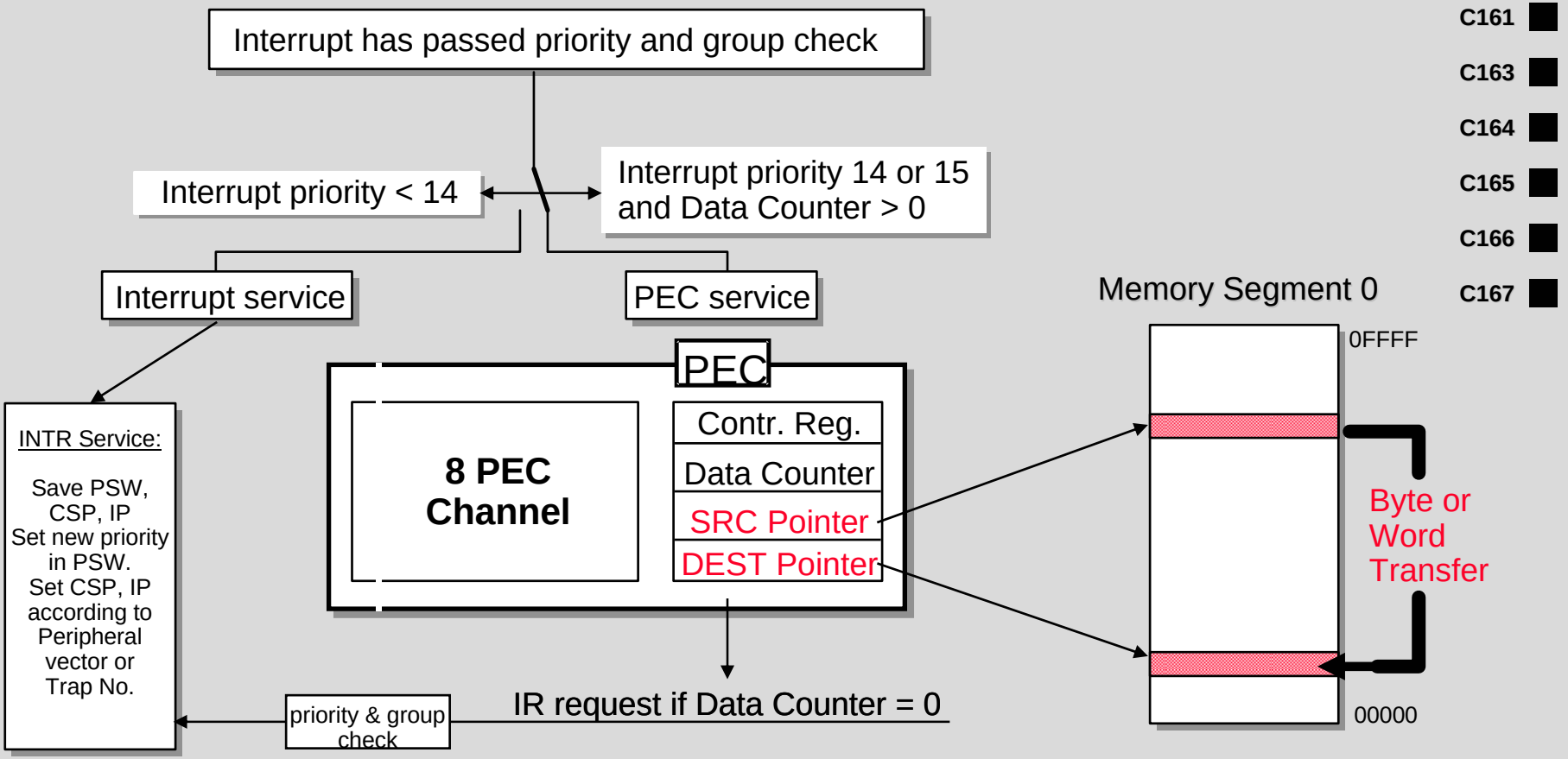


*** External Interrupts are possible, e.g. instead of the Capture Input**

55 Peripheral Interrupts

36 ext. Interrupts(+ NMI) including 8 which are sampled every 50 ns

Peripheral Event Controller (PEC)



Peripherals Set of the C167...

- **2 General Purpose Timer units (GPT1 & GPT2)**
  - 5 Timers (200/400ns) with enhanced Input/Output, Reload and Capture functions and complex concatenation capabilities
- **2 Capture/Compare units (CAPCOM1 & 2)**
  - 4 Timers (400ns) with Reload register and 32 independent 16-bit Capture/Compare channels programmable to 6 modes of operation
- **4 high resolution PWM channels**
  - each with independent time-base of up to 50ns resolution and programmable operation modes (edge-aligned, center-aligned, burst and single-shot mode)
- **...**

C161
C163
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C166
C167

...Peripherals Set of the C167

- **Independent USART**
  - max 625 KBaud asynchronous and max 2.5 Mbit/sec synchronous data transfer
- **Fast Serial Synchronous Communication interface (SSC)**
  - max 5 Mbit/sec full duplex transfer rate, SPI compatible
- **Fast and accurate A/D Converter**
  - 10-Bit resolution, 16 input channels, 9.7µs conversion time, enhanced continuous and scan modes with channel-injection capability.
- **I/O Ports**
  - 8 Ports provide 111 I/O lines
- **Watchdog: 16-Bit Reload-timer causes reset on overflow**

C161
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General Purpose Timer 1(GPT 1) at 20 MHz

- **Three 16-bit up/down timers: 2 auxiliary timers(T2,T4) and 1 core timer(T3)**
- **Input mode**
  - Timer mode: Internal clock input with prescaler up to 2.5 MHz / 400 ns; Clock can be gated with external signal
  - Counter Mode: external clock up to 1.25 MHz
  - Cascading of core timer and any aux. timer (33-Bit timer)
- **Count direction (only T3) can be changed externally**
- **Output mode**
  - Interrupt possibility and toggle function at the core timer T3
  - Interrupt possibility at auxiliary timers T2 and T4
- **Reload: Core timer can be reloaded with the contents of any aux. timer**
- **Capture: Contents of the core timer can be latched into any aux. timer**

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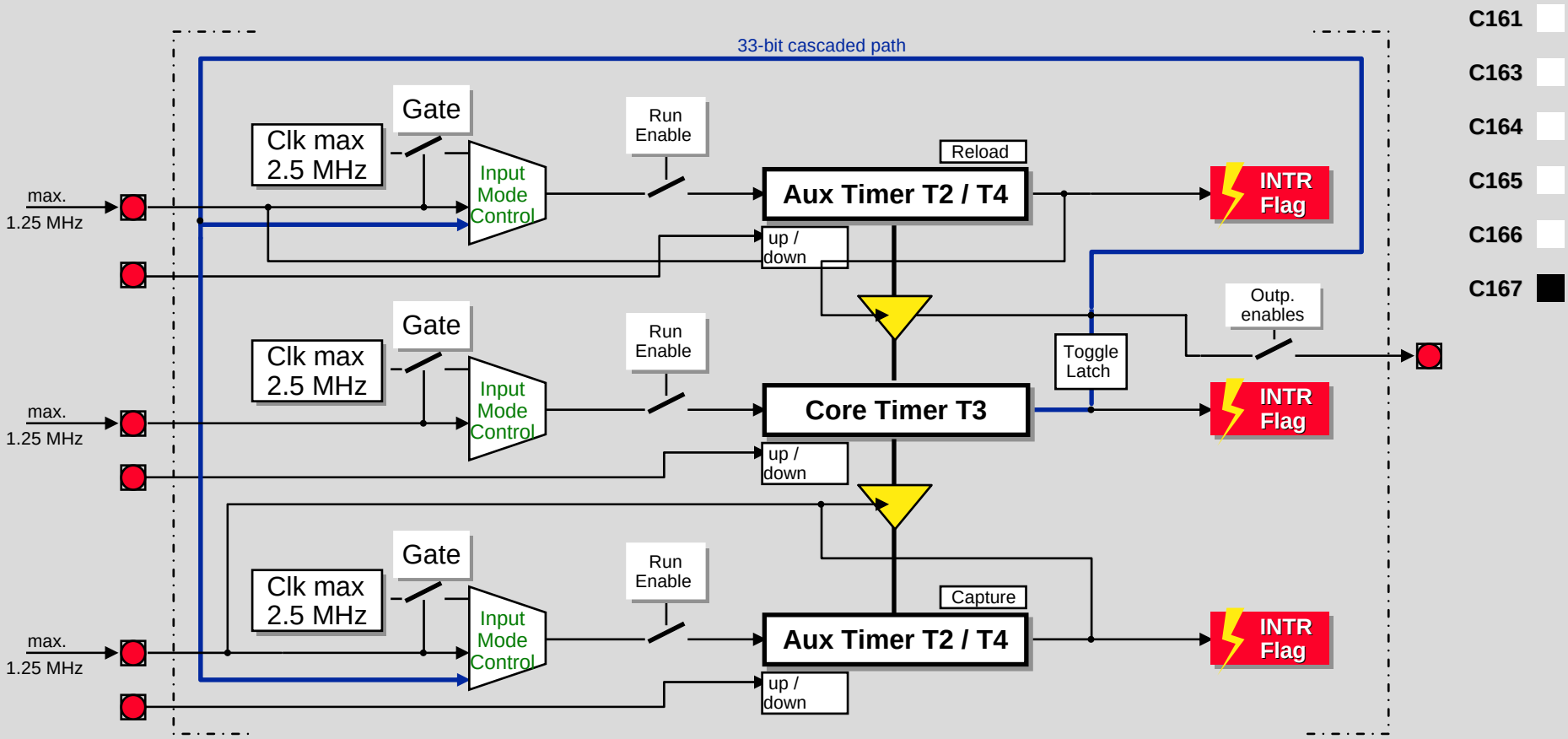
GPT 1 Function Diagram at 20 MHz



General Purpose Timer 2 (GPT 2) at 20 MHz

- **Two 16-Bit up/down timers (T5, T6)**
- **Input mode**
  - Timer mode: Internal clock input with prescaler up to 5MHz (200ns)
  - Counter mode: External clock up to 2.5 MHz
  - T5 can also be clocked with the toggle bit of T6
- **Output mode**
  - Interrupt possibility and toggle function of a port line (via a toggle bit)
  - Output of T6 can be used to clock CAPCOM timers
- **Count direction of all timers can be dynamically changed (C167)**
- **Cascading of timer T6 with timer T5**
- **One 16-Bit Capture(for T5) / Reload(for T6) register**
  - Reload register for T6, Capture register for T5

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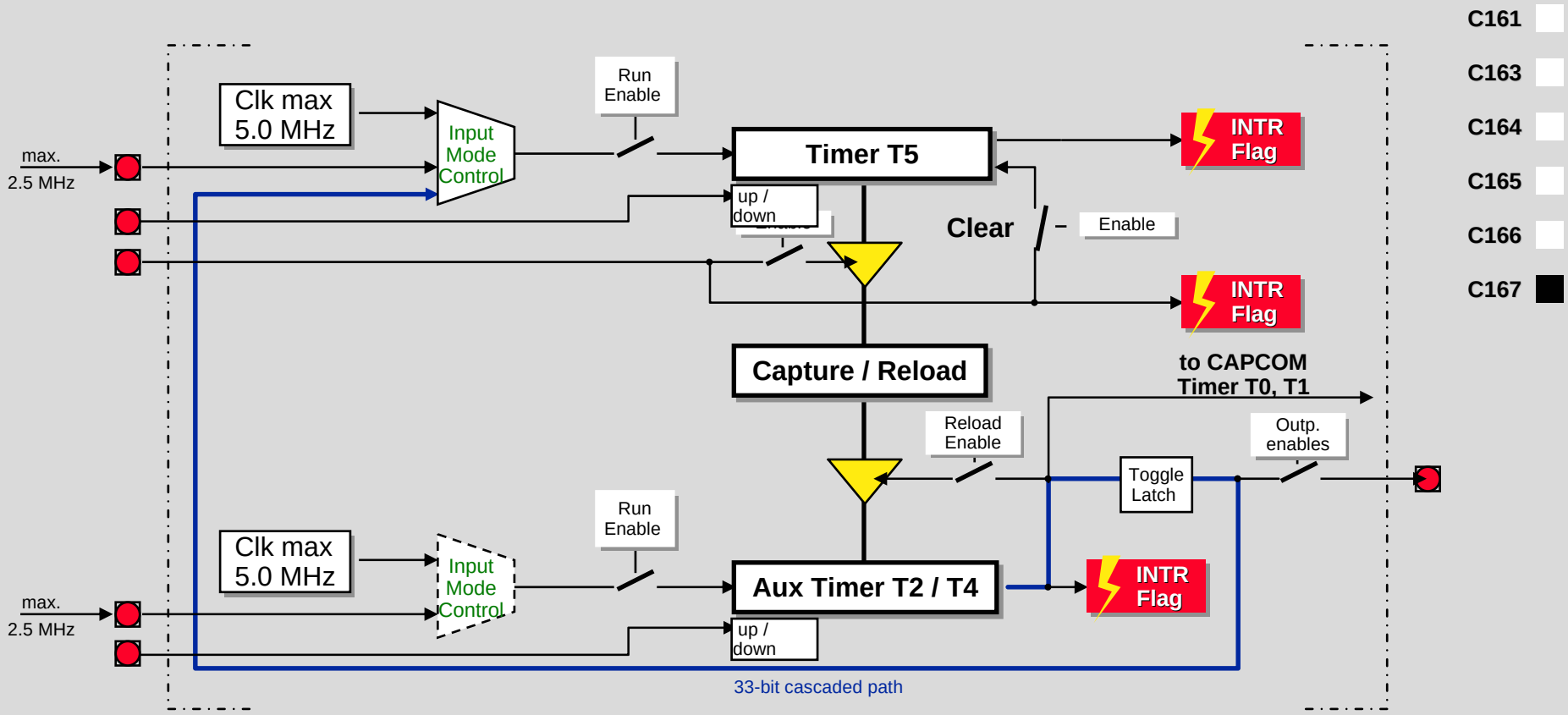
GPT 2 Function Diagram at 20 MHz



Capture / Compare Unit 1/2 (CAPCOM 1/2)...

- **Four 16-bit timers (T0/T1 & T7/T8), 16-bit reload reg. each**
  - **Timer mode:** Int. clock input with up to 2.5 MHz (400ns)
  - **Counter mode:** External clock input to T0/T7 up to 1.25 MHz, Output from T6 can be used as clock input
  - CAPCOM 2 can be synchronized via T0 to CAPCOM 1
- **Two units with sixteen 16-Bit Capture/Compare registers**
  - Individually program. for Capture or any Compare mode
  - Individually allocatable to timer T0/T1 or T7/T8
- **Various Compare modes for flexible Pulse Width Modulation(PWM)**
  - Output-Pin toggles if Compare is true
  - 1 or 2 Compare registers can operate to one Output-Pin
  - One or more Compare events can be detected in one timer period
  - Interrupt only mode

C161
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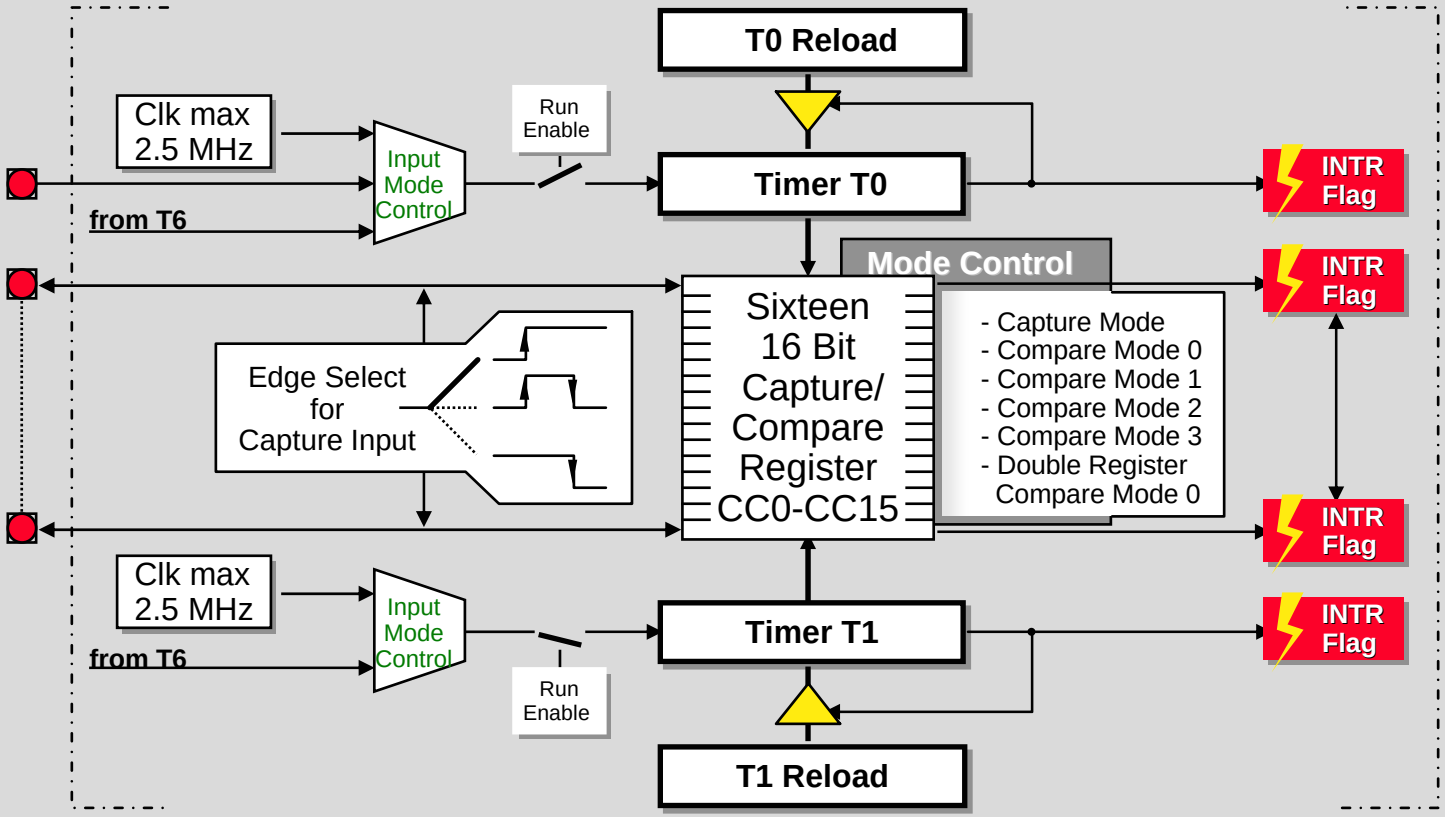
CAPCOM(1) Function Diagram



C161
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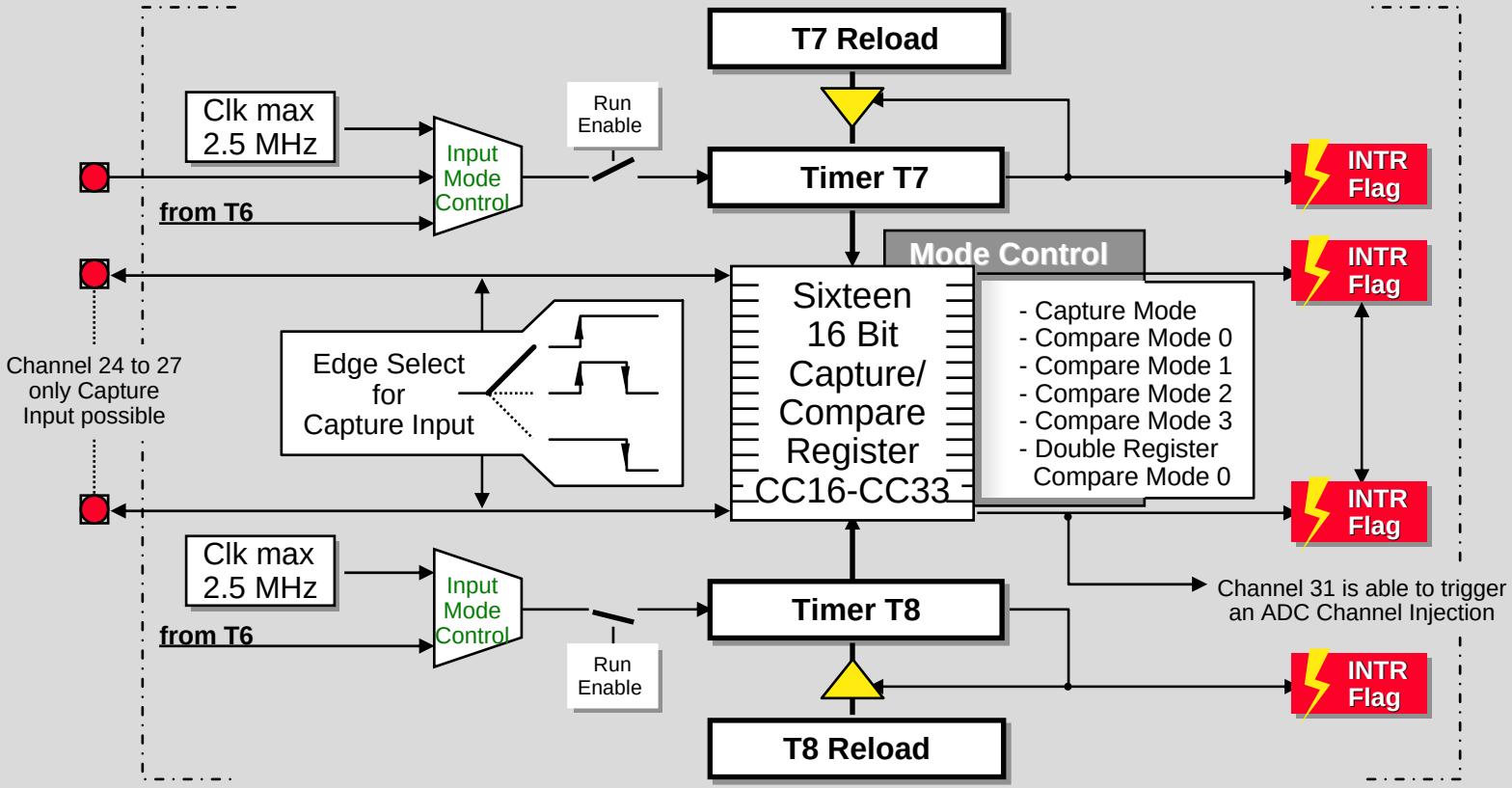
CAPCOM 2
Function Diagram



C161
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CAPCOM 1/2
Compare Mode 0 and 1

- **Several Compare events are possible within a single Timer period**

C161
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C166
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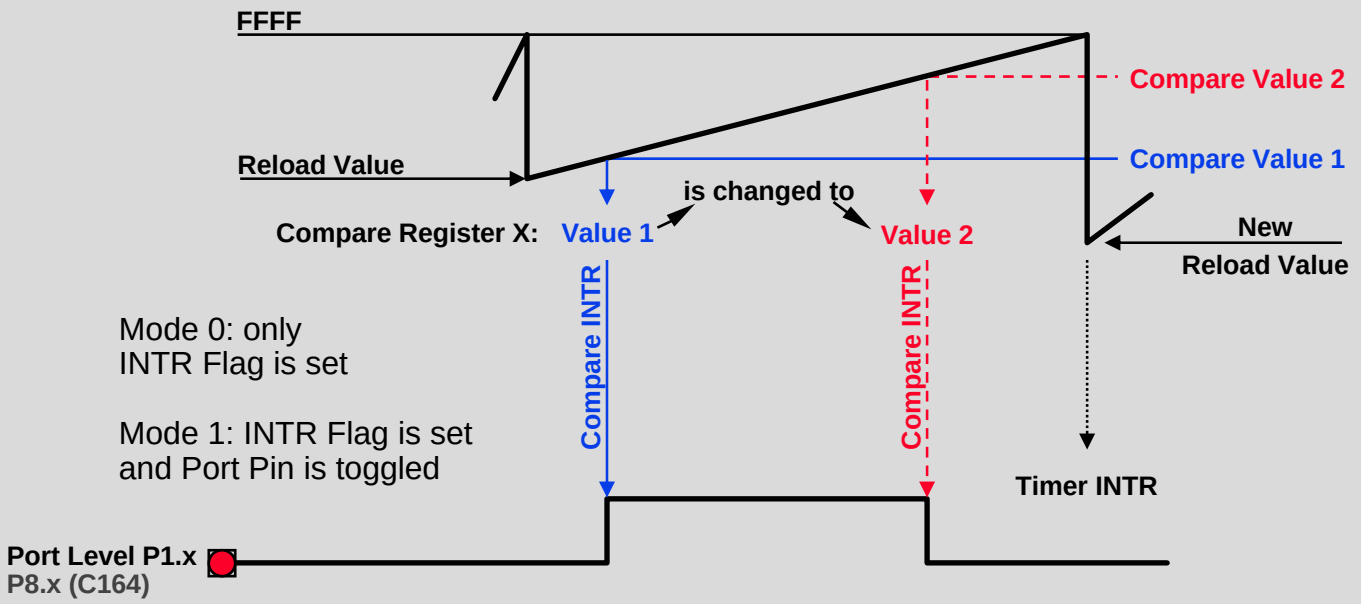

CAPCOM 1/2
Compare Mode 2 and 3

- **Only one Compare events is possible within a single Timer period**

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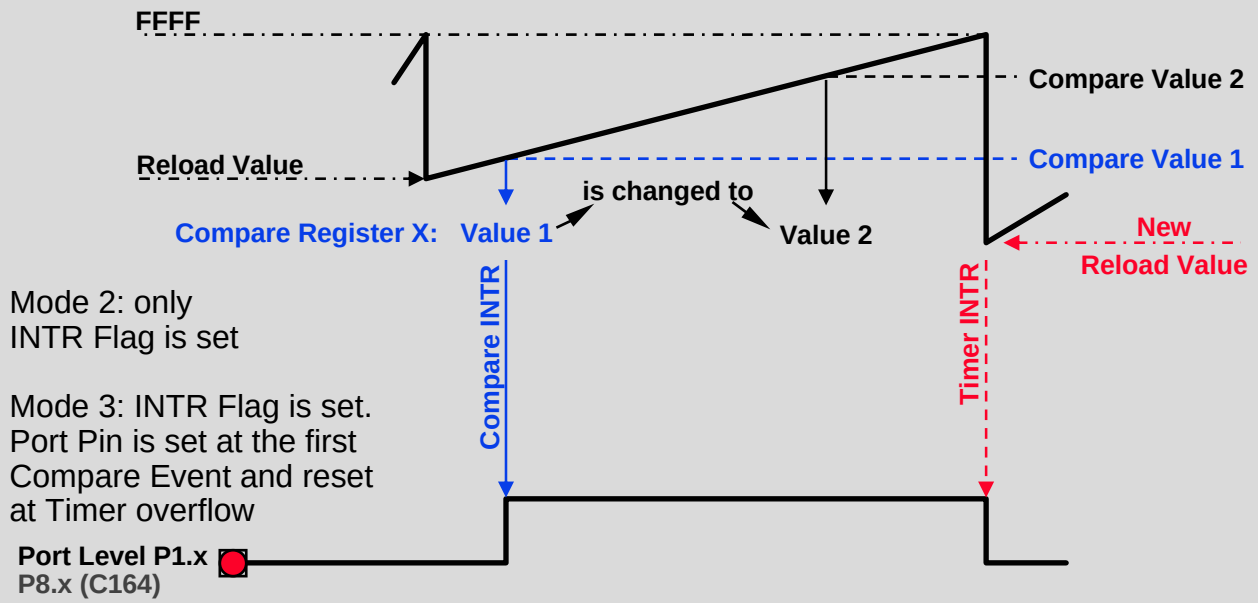

CAPCOM 1/2
Double Register Compare Mode

- **Two Compare Register work together to control one Port Pin**
- **This mode is selected by a special combination of the mode 0 and 1**

C161
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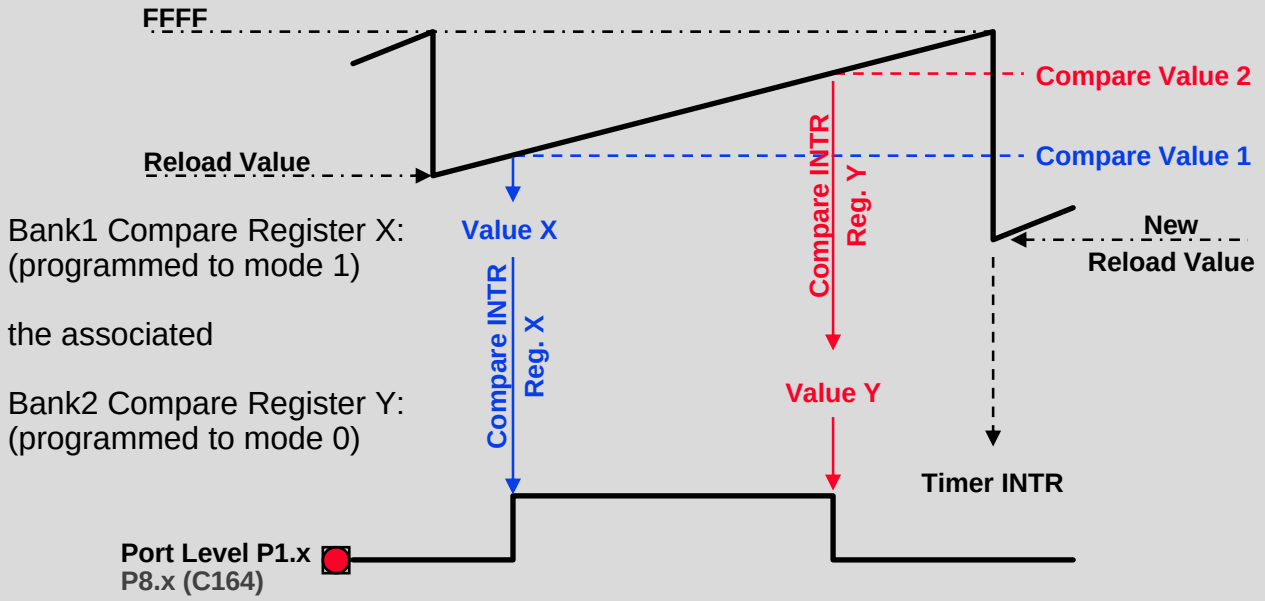
C166
C167



Pulse Width Modulation Unit (PWM)

- **4 completely indep. PWM channels each with its own time-base**
  - 50ns or 12.8µs timer-resolution provides a very wide frequency range to generate PWM signals
  - Programmable output polarity
  - Up to 78 KHz at 8-bit PWM resolution

$$F_{PWM} = \frac{1}{2^{8\text{-bit}} \times 50ms} = 78\ KHz$$

- **Four operation modes**
  - Standard, edge-aligned PWM
  - Symmetrical, center-aligned PWM for asynchronous motor control
  - Burst-mode for modulated PWM signals
  - Single-shot mode

C161
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PWM unit
Frequencies and Resolution

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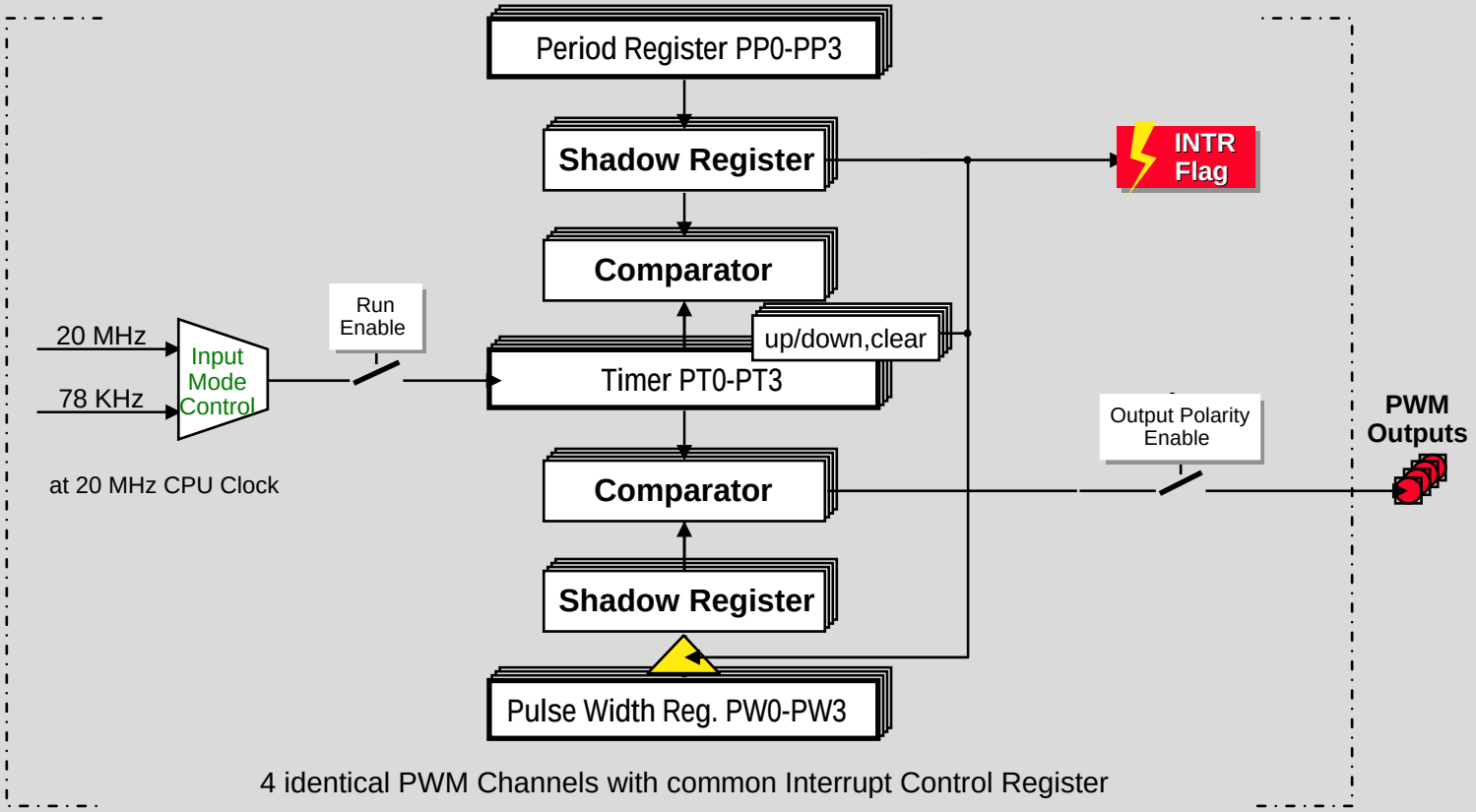
PMW Unit Frequencies and Resolution in Mode 0 Operation (EDGE-ALIGNED)

Resolution → / ↓ Input Clock (CPU @ 20 MHz)	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
CPU Clock (50ns Resolution)	78.1 KHz	19.5 KHz	4.88 KHz	1.22 KHz	305 Hz
CPU Clock / 64 (3.2µs Res.)	1.22 KHz	305 Hz	76.3 Hz	13.1 Hz	4.77 Hz

PMW Unit Frequencies and Resolution in Mode 1 Operation (SYMMETRICAL)

Resolution → / ↓ Input Clock (CPU @ 20 MHz)	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
CPU Clock (50ns Resolution)	39.1 KHz	9.77 KHz	2.44 KHz	610 Hz	152.6 Hz
CPU Clock / 64 (3.2µs Res.)	610 Hz	152.6 Hz	38.15 Hz	9.54 Hz	2.4 Hz

PWM unit
Function Diagramm



4 identical PWM Channels with common Interrupt Control Register

C161
C163
C164
C165
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PWM unit
Mode 0 and 1...

C161
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C164
C165
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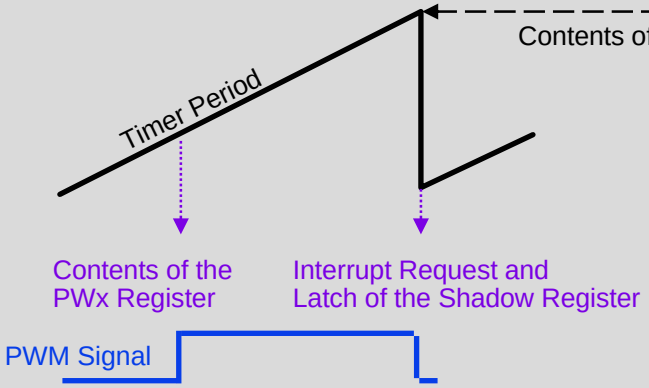
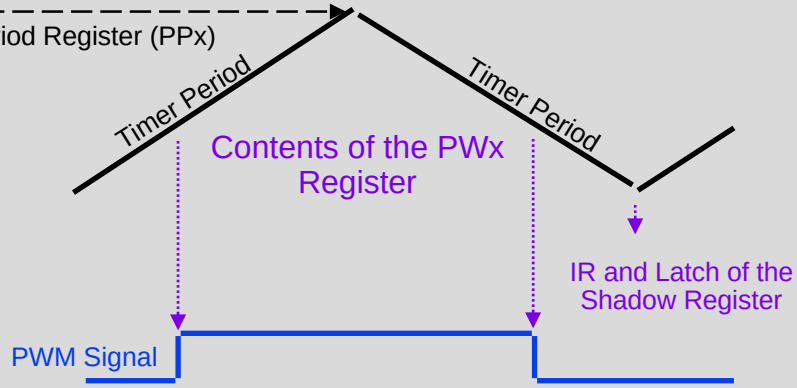
PWM Mode 0:
Standard PWM's or Edge-Aligned PWM's



If all channels are programmed to **mode 0**,
edge-aligned PWM signals will be generated.
A duty cycle from **0 to 100%** is programmable

PWM Mode 1:
Symmetrical or Center-Aligned PWM's

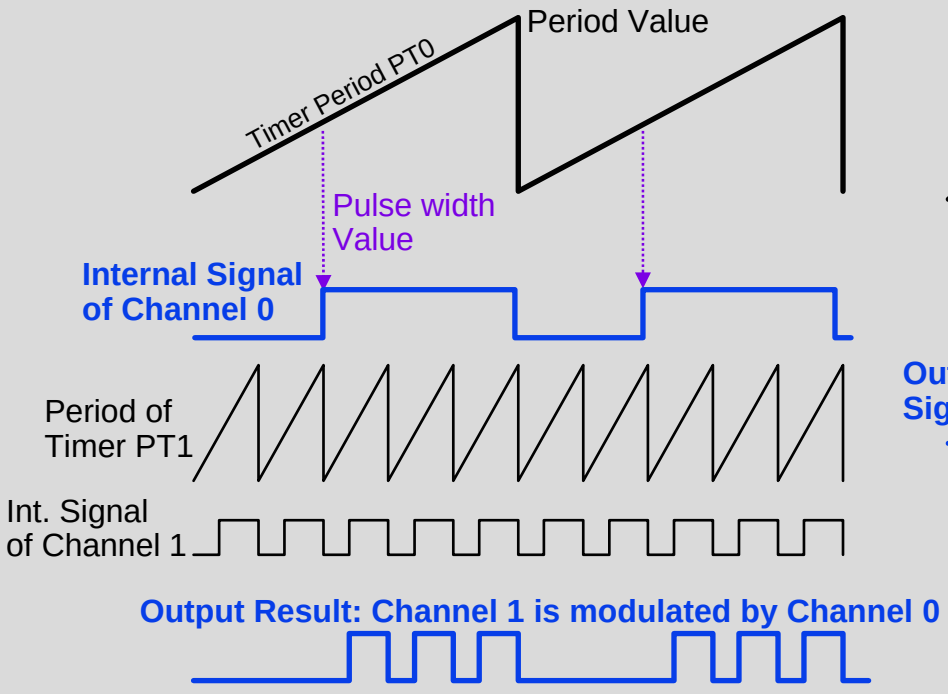


If all channels are programmed to **mode 1**,
center-aligned PWM signals will be generated.
A duty cycle from **0 to 100%** is programmable

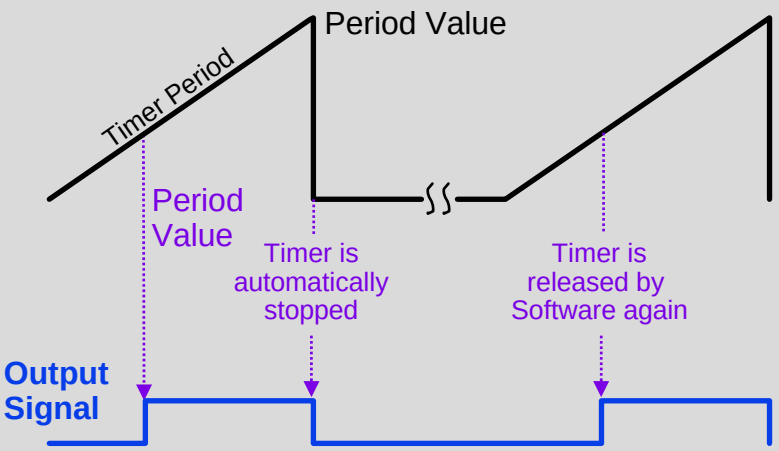
Possible PWM Signals from other channels programmed to the same mode:

... PWM unit Modes

Burst Mode :
Burst Sequence by combining PWM channel 0 and 1



Single Shot :
Only one PWM Pulse is generated
Mode available for channel 2 and 3



The Timer can be dynamically changed to lengthen (retrigger) or shorten the output pulse

C161
C163
C164
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C167

Analog Digital Converter (ADC)

- **10-Bit ADC based on the successive approximation principle**
  - 9.7µs conversion-time
  - On-chip sample- & hold-circuit (1.6 us sample-time)
  - 16 Multiplexed input channels
  - Automatic self-calibration after conversion
- **Flexible operation mode**
  - Single-channel and single-channel-continuous for periodic data acquisition
  - Auto-scan and auto-scan-continuous for permanent data tracking
  - Channel-injection mode with own result-register can be used to interrupt the scan modes
- **Easy error handling and channel identification**
  - 10-bit result and channel number in result register
  - Overrun error check

C161
C163
C164
C165
C166
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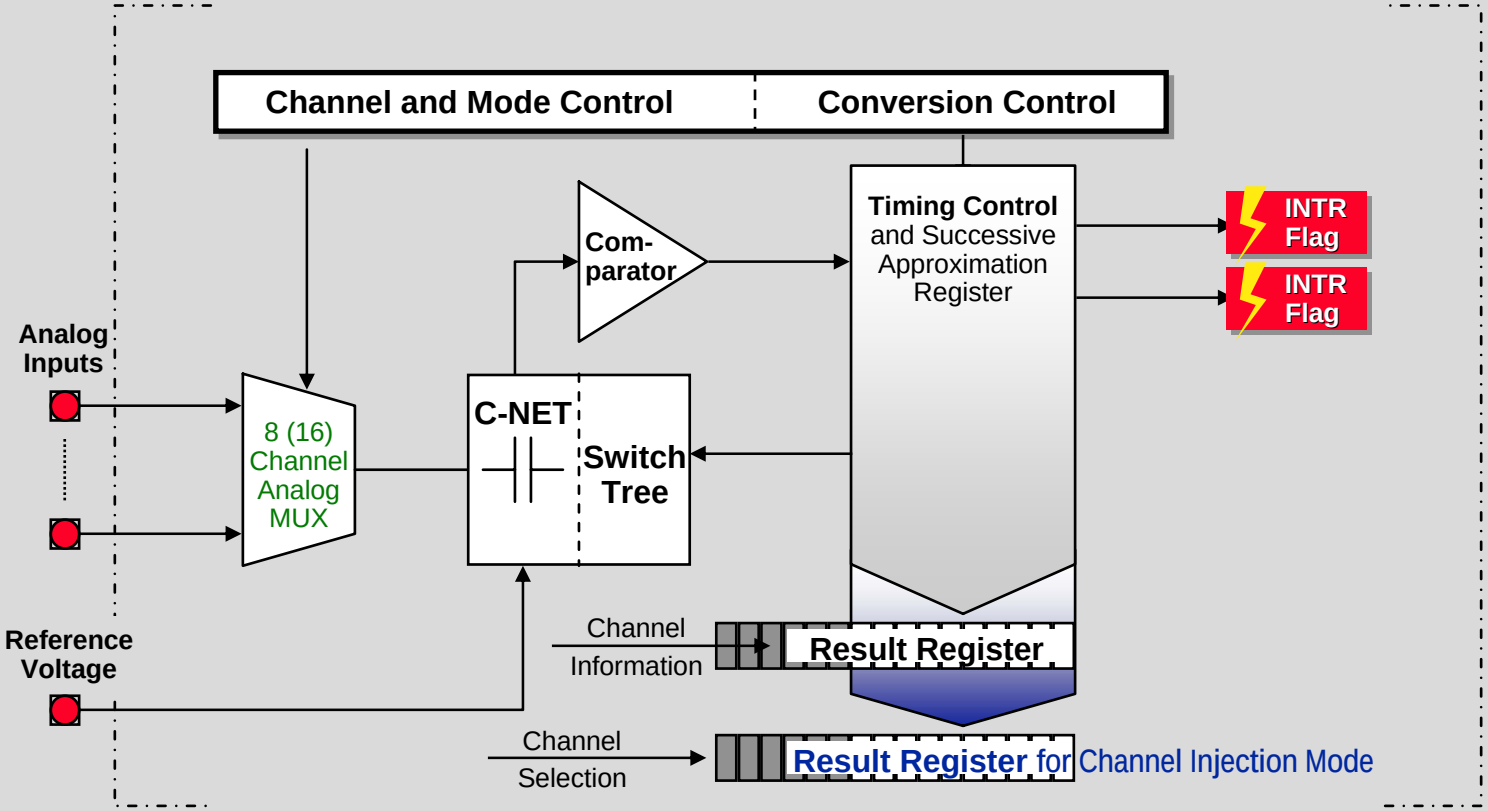
10-Bit A/D Converter Block Diagram

C161
C163
C164
C165
C166
C167



Asynchronous / Synchronous Serial Channel (USART) at 20MHz

C161
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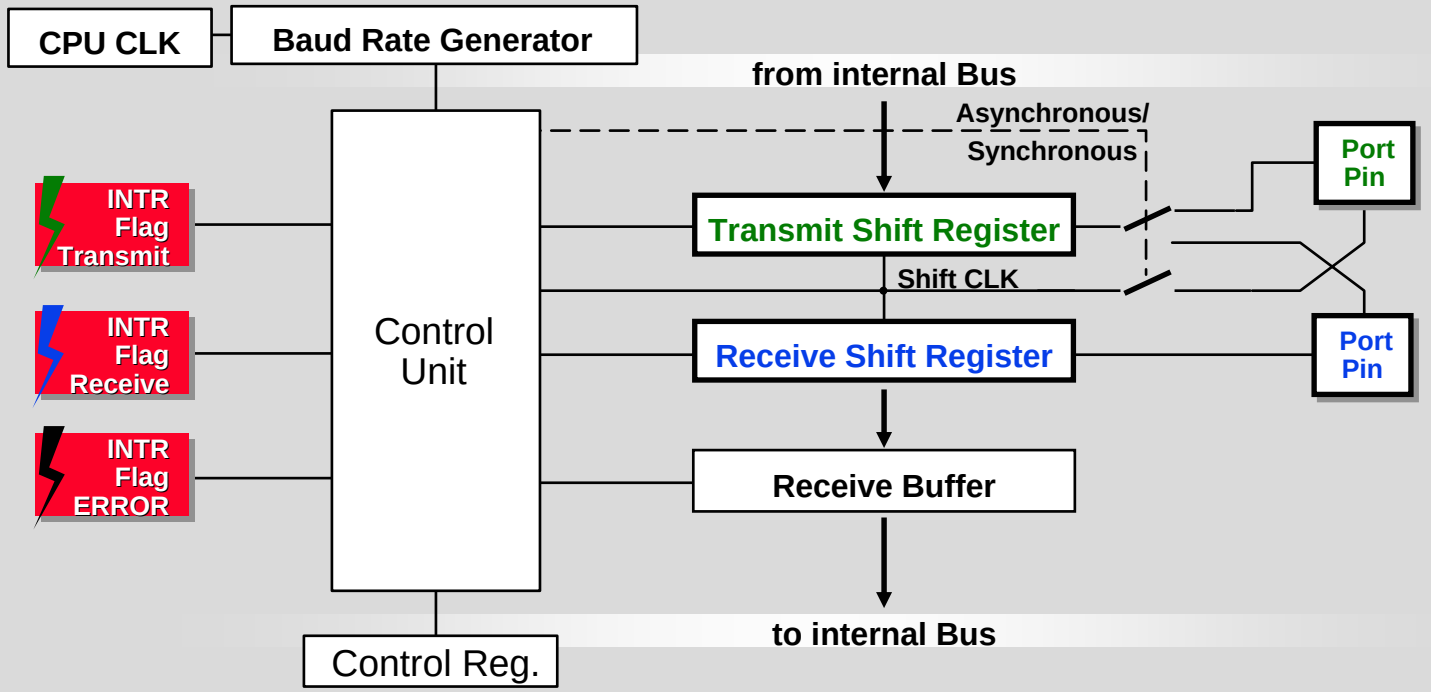
- **Synchronous / asynchronous serial channel with its own baud-rate-generator**
- **Asynchronous mode with max 625 KBaud transfer rate**
  - Full duplex (receive and transmit at the same time)
  - programmable features:
  - 1 or 2 stop bits, 7, 8 or 9 data bits
  - Generation of parity- or wake-up bit at data transmission
  - Odd or even parity
  - Error detection (parity, overrun, framing)
  - Wake-up check (receive int. flag is set if wake-up bit is true)
- **Synchronous mode with max 2.5 Mbit/sec transfer range**
  - Half duplex operation (only transmit or receive possible)
  - Easy I/O expansion with external shift register
  - Overrun error detection

USART
Block Diagram

C161
C163
C164
C165
C166
C167

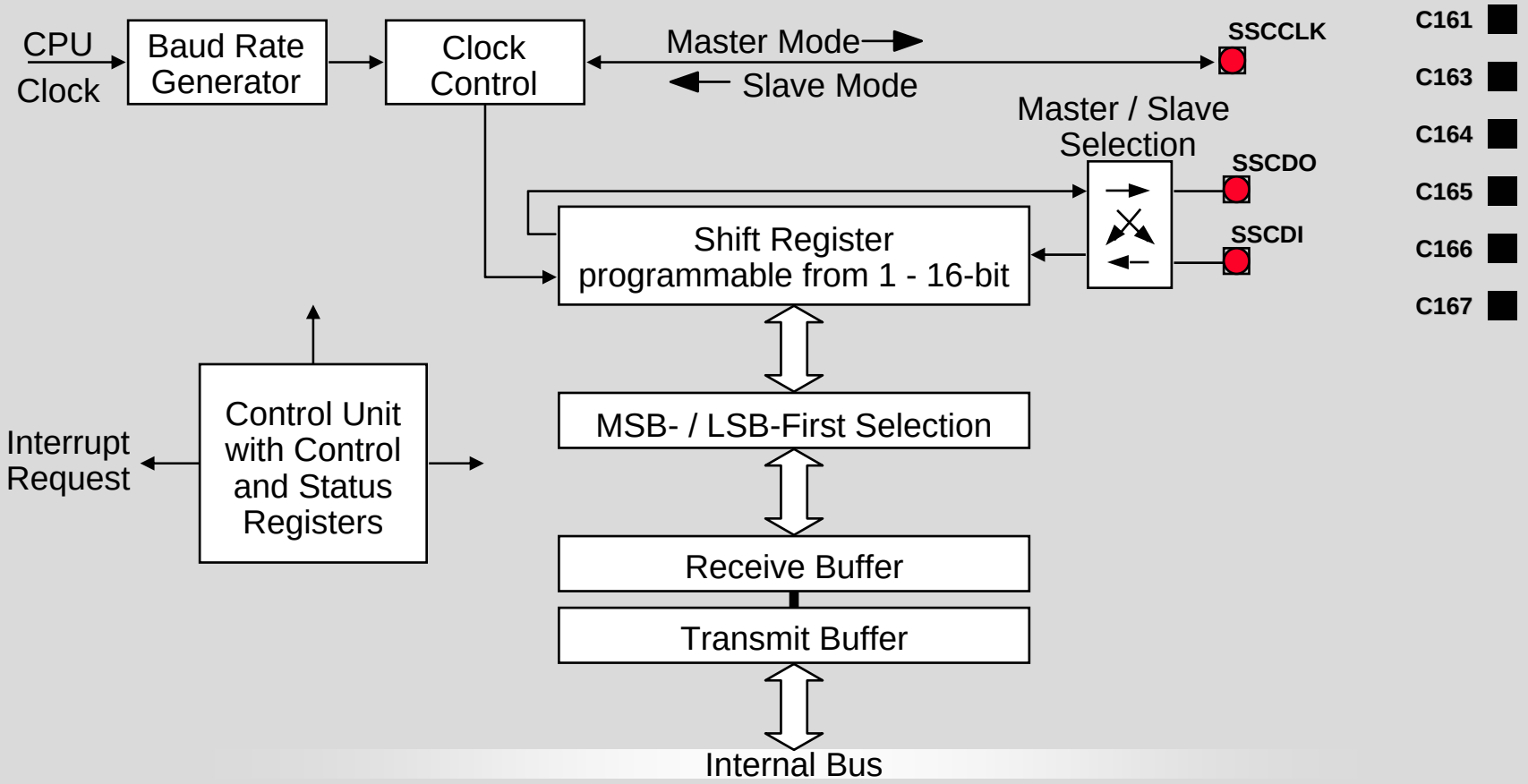


Synchronous Serial Channel (SSC), SPI compatible at 20 MHz

- **Full duplex Synchronous Serial Channel (SSC) with its own baudrate generator for high speed communication**
- **Up to 5 Mbit/sec transfer rate**
- **SPI compatible**
- **Master (clock is output) or slave mode (clock is input)**
- **Programmable features to satisfy various communication requirements**
  - MSB or LSB first
  - Data frame from one to 16-bit
  - Clock polarity and phase

C161	
C163	
C164	■
C165	
C166	■
C167	■

Synchronous Serial Channel - Block Diagram



Differences between SSP and SSC

SSP (C163) Synchronous Serial Port	SSC Synchronous Serial Channel
Up to 10 MBaud @ 20 MHz CPU clock	Up to 5 MBaud @ 20 MHz CPU clock
Only half duplex communication possible; one bidirectional data line	Full duplex communication possible; two data lines (Transmit, Receive)
Shift clock can only be generated (master only)	Shift clock can be generated (master) or received (slave)
Data width 1 byte	Data width can be chosen from 2 bits to 16 bits
No error detection mechanisms	Error detection mechanisms
Two dedicated chip enable lines	No dedicated chip enable lines
Connected to XBUS	Connected to Internal Bus
1 interrupt source dedicated to SSP	3 interrupt sources dedicated to SSC

C161 ■
C163 ■
C164 ■
C165 ■
C166 □
C167 ■

User Benefits...

- **CAN is low cost**
  - Serial bus with two wires: good price/performance ratio
  - Low cost protocol devices available driven by high volume production in the automotive and industrial markets
  - About 15.000.000 CAN nodes in use so far
- **CAN is reliable**
  - Sophisticated error detection and error handling mechanisms results in high reliability transmission
  - Example: 500 kbit/s, 25% bus load, 2000 hours per year: One undetected error every 1000 years
  - Erroneous messages are detected and repeated
  - Every bus node is informed about an error
  - High immunity to Electromagnetic Interference
- **...**

C161
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...User Benefits...

- **CAN means real-time**
  - Short message length (0 to 8 data bytes / message)
  - Low latency between transmission request and actual start of transmission
  - Inherent Arbitration on Message Priority (AMP)
  - Multi Master using CSMA/CD + AMP method
- **CAN is flexible**
  - CAN Nodes can be easily connected / disconnected (i.e. plug & play)
  - Number of nodes not limited by the protocol
- **CAN is fast**
  - maximum data rate is 1 MBit/s @ 40 m bus length (still about 40 kBit/s @ 1000 m bus length)
- **...**

C161
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...User Benefits

- **CAN allows Multi-Master Operation**
  - Each CAN node is able to access the bus
  - Bus communication is not disturbed by faulty nodes
  - Faulty nodes self swith-off from bus communication
- **CAN means Broadcast Capability**
  - Messages can be sent to single/multiple nodes
  - All nodes simultaneously receive common data
- **CAN is standardized**
  - ISO-DIS 11898 (high speed applications)
  - ISO-DIS 11519-1 (low speed applications)

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Application Examples...

- **CAN in motor vehicles (cars, trucks, buses)**
  - Enables communication between ECUs like engine management system, anti-skid braking, gear control, active suspension ... (power train)
  - Used to control units like dashboard, lighting, air conditioning, windows, central locking, airbag, seat belts etc. (body control)
- **CAN in utility vehicles**
  - e.g. construction vehicles, forklifts, tractors etc.
  - CAN used for power train and hydraulic control
- **...**

C161
C163
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...Application Examples...

- **CAN in trains**
  - High need of data exchange between the different electronic subsystem control units
  - Mainly data about acceleration, braking, door control, error messages etc. but also for diagnosis
- **CAN in industrial automation**
  - Excellent way of connecting all kinds of automation equipment (control units, sensors and actuators)
  - Used for initialization, program and parameter up-/download, exchange of rated values / actual values, diagnosis etc.
  - Machine control (printing machines, paper- and textile machines etc.): Connection of the different intelligent subsystems
  - Transport systems
- **...**

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...Application Examples

- **CAN in medical equipment**
  - Computer tomographs, X-ray machines, dentist chairs, wheel chairs
- **CAN in building automation**
  - Heating, air conditioning, lighting, surveillance etc.
  - Elevator and escalator control
- **CAN in household appliances**
  - Dishwashers, washing machines, even coffee machines...
- **CAN in office automation**
  - photo copier, interface to document handler, paper feeding systems, sorter
  - communicates status, allows in field connection or "hot swapping"
  - DocuText Systems, i.e. automatic print, sort and bind on demand

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Some things worth knowing about CAN...

- Developed in the mid-eighties by BOSCH
- Asynchronous serial bus with linear bus structure and equal nodes (Multi Master bus)
- CAN does not address nodes (address information is inside the messages combined with message priority)
- Two bus states: dominant and recessive
- Bus logic according to "Wired-AND" mechanism: dominant bits (Zeros) override recessive bits (Ones)
- Bus Access via CSMA/CD with NDA (Carrier Sense Multiple Access/ Collision Detection with Non-Destructive Arbitration)

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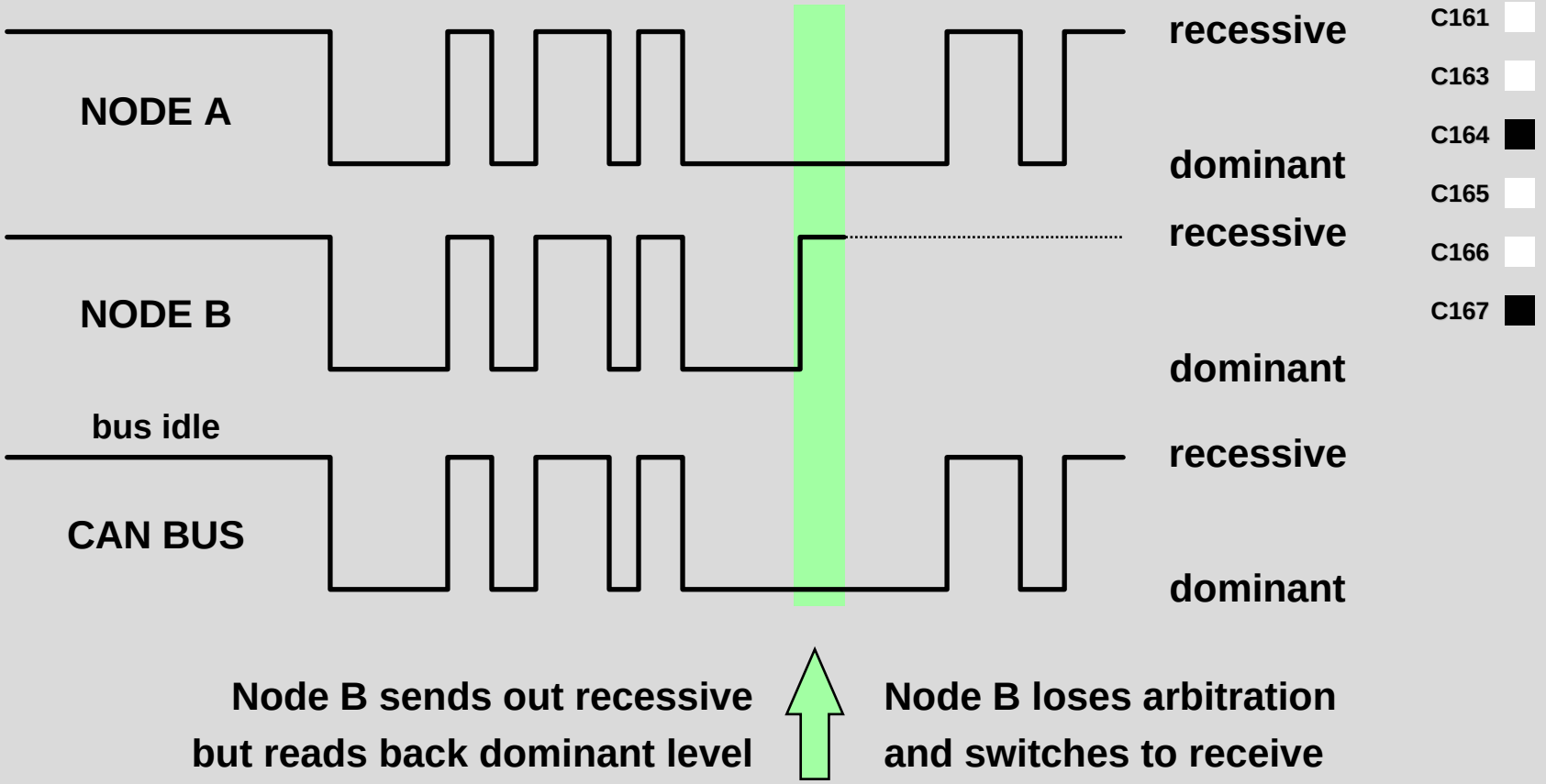
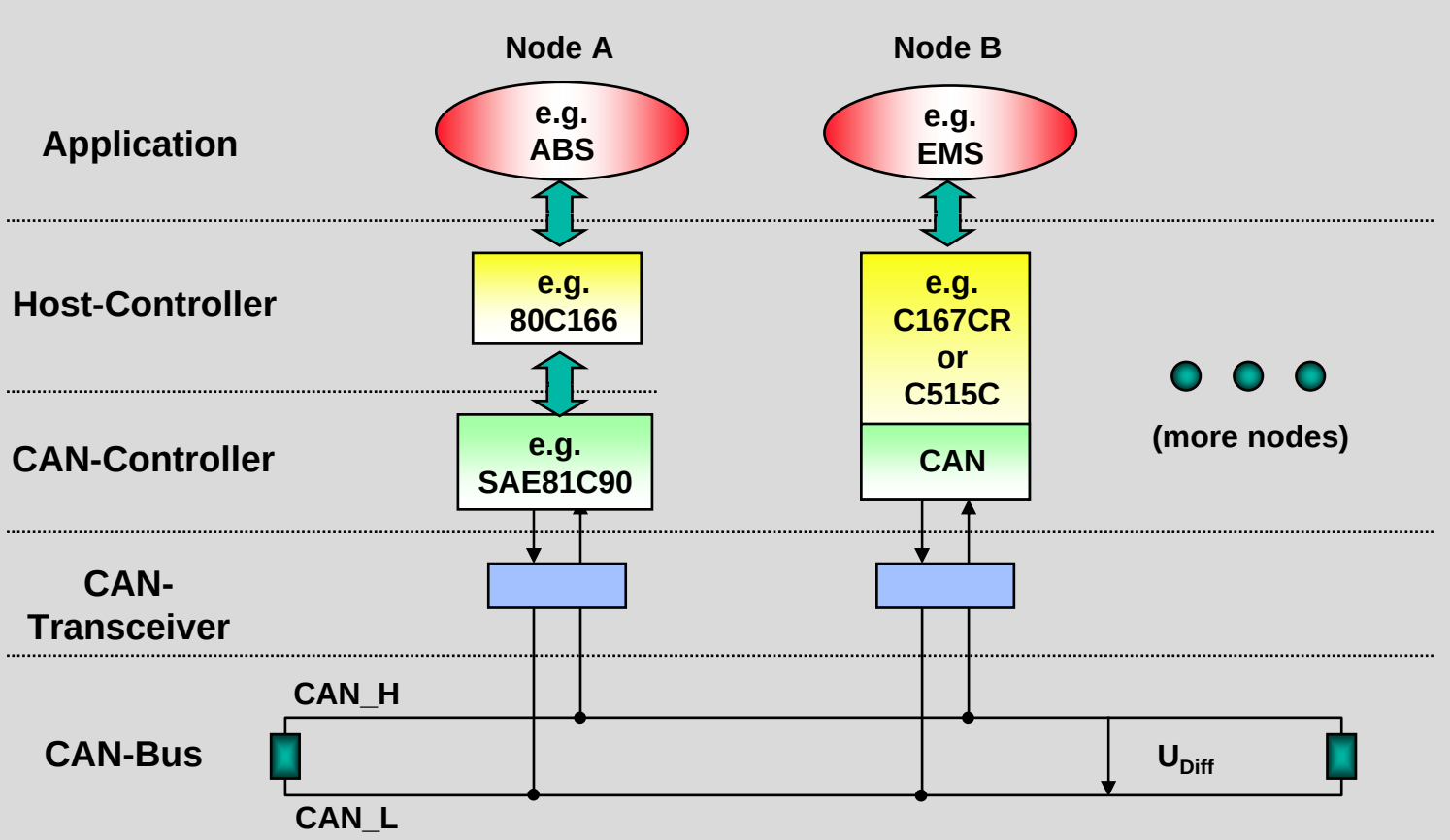
...Some things worth knowing about CAN



Typical CAN node structure



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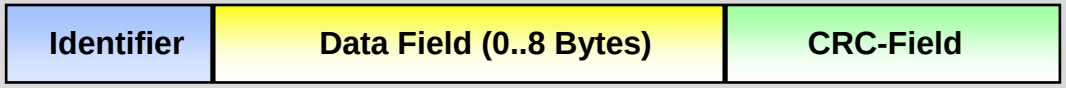
CAN Data Frames...

- **There are mainly two ways of communicating:**
  - One node is 'talking', all other nodes 'listen'
  - Node A is asking Node B for something and gets the answer.
- **To 'talk', CAN nodes use *Data Frames*.**
  - A Data Frame consists of an Identifier, the data to be transmittedand a CRC-Checksum.



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...CAN Data Frames

- The identifier specifies the contents of the message ('engine speed', 'oil temperature', etc.) and the message priority
- The Data Field contains the corresponding value ('6000 rpm', '110°C', etc.)
- The Cyclic Redundancy Check is used to detect transmission errors.
- All nodes receive the Data Frame. Those who do not need the information, just don't store it.

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CAN Basics...

- **To 'ask' for information, CAN nodes use *Remote Frames*.**
  - A Remote Frame consists of the Identifier and the CRC-Checksum.
    It contains no data.

  - The identifier contains the information that is requested ('engine speed', 'oil temperature', etc.) and the message priority.
  - The node that is supposed to provide the requested information
    (e.g. the sensor for the oil temperature) does so by sending the corresponding Data Frame (same identifier, the Data Field contains the desired information).

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...CAN Basics

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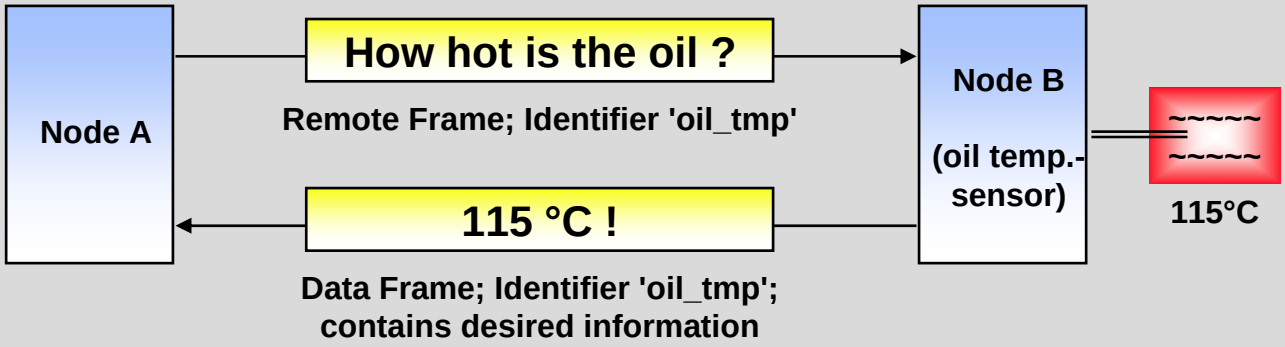

Standard CAN / Extended CAN...

- **Most CAN nodes talk in the 'language' that most other CAN nodes understand: They use *Standard* Data or Remote Frames.**
  - A Standard Frame contains an identifier which is 11 bits long.
  - With this 11 bits, 2^{11} (=2048) different messages can be addressed.
  - CAN nodes using Standard-CAN-Frames use the CAN Specification Version 2.0A.
- **Some CAN nodes talk with a special 'accent': They use *Extended* Data or Remote Frames.**
  - An Extended Frame contains an identifier which is 29 bits long.
  - ...

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...Standart CAN / Extended CAN...

- Over 536 million (2^{29}) different messages can be addressed.
- CAN nodes using Extended-CAN-Frames use the CAN Specification Version 2.0B (active).

- **Some Standard-CAN nodes don't understand this 'accent', but they tolerate it and just don't care.**
  - If an Extended Frame is 'on the air', these CAN nodes cannot store the data, but they as well do not produce errors.
  - These CAN nodes use CAN Version 2.0A, but are also known as Version 2.0B passive.
  - They can be used in a Controller Area Network where Extended Frames are used.
- **...**

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...Standart CAN / Extended CAN

- **Some Standard-CAN nodes don't understand and also don't tolerate this 'accent'.**
  - If an Extended Frame is 'on the air', these CAN nodes produce errors.
  - These CAN nodes use only CAN Version 2.0A.
  - They can *not* be used in a Controller Area Network where Extended Frames are used.

- **SIEMENS 16 bit parts: C167CR, C164CI: V2.0B active**

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Basic CAN / Full CAN...

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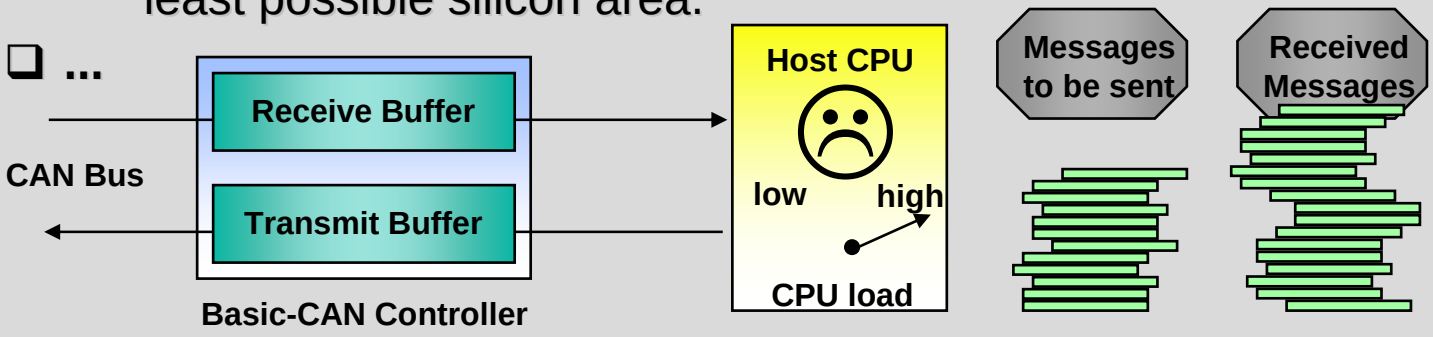
- **In some CAN controllers, only the basic CAN functions are implemented. They are called *Basic-CAN* controllers.**
  - Mostly there's only one transmit buffer and one or two receive buffers for transmission and reception of the Data- / Remote Frames.
  - Each incoming message is stored. The host CPU has to decide whether the message data is needed or not.
  - Therefore these controllers should only be used in CANs with very low baudrates and/or very few messages because of the high CPU load. Advantage: They use the least possible silicon area.
- ...



...Basic CAN / Full CAN...

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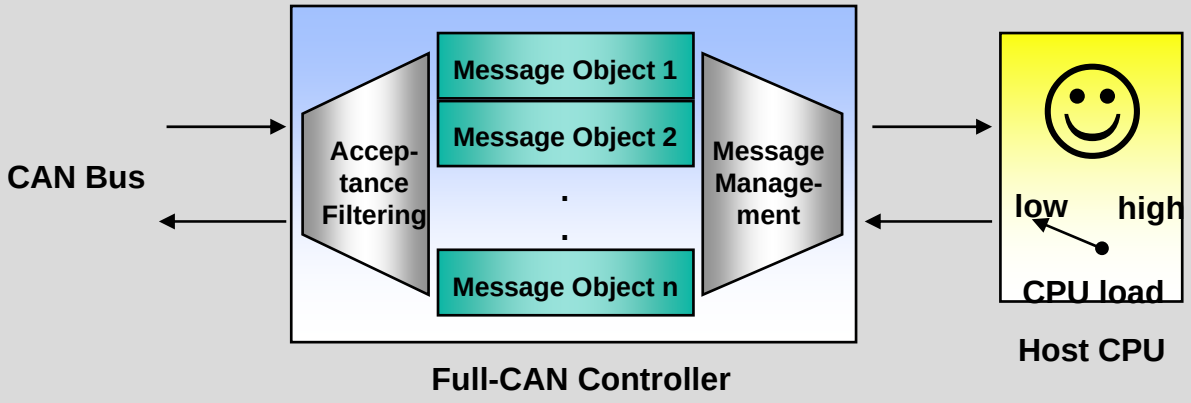
- **In the other CAN controllers, also message management and acceptance filtering are implemented. They are called *Full-CAN* controllers.**
  - There are several Message Objects, each with its own identifier.
  - Only if a message for one of these preprogrammed identifier is received, it is stored and the CPU is interrupted.
  - In this way, the CPU load is low.
- **...**



...Basic CAN / Full CAN

- **All Siemens CAN-Controllers are Full-CAN controllers. But they also provide Basic-CAN functionality**
  - one message object can be used like a Basic CAN receive register

C161
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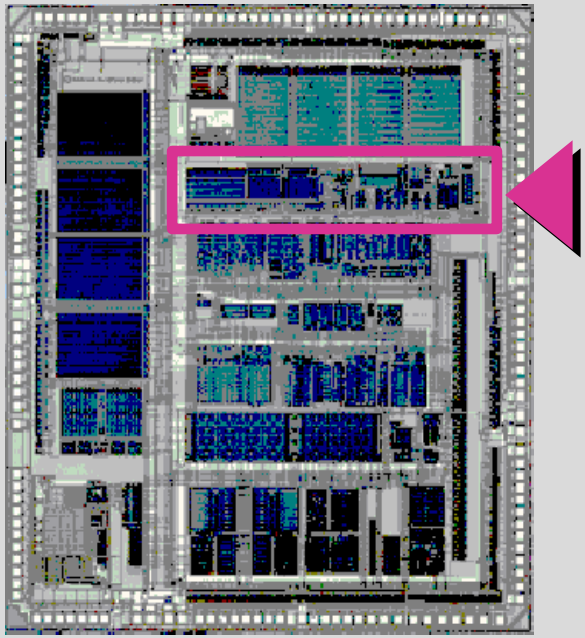
Features of the CAN Module on C167CR / C164CI...

- **Functionality corresponds to AN 82527**
- **Complies with CAN spec V2.0B active (Standard- und Extended-CAN)**
- **Maximum CAN Transfer Rate (1 MBit/s)**
- **Full CAN Device**
  - 15 Message Objects with their own identifier and their own status- and control bits
  - Each Message Object can be defined as Transmit- or Receive Object
- **...**



C161
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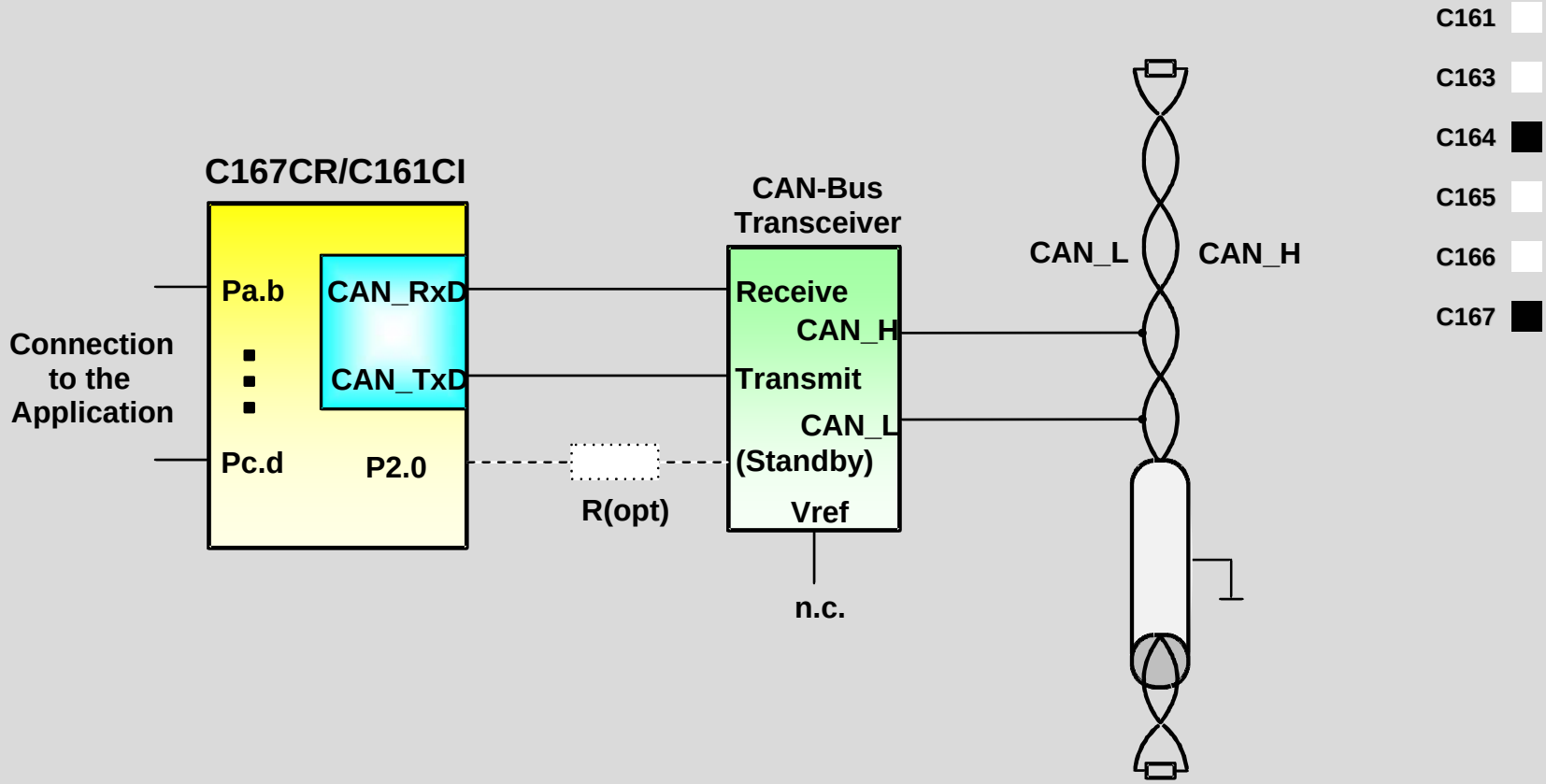
Connecting the to CAN



Watchdog Timer (WDT) at 20 MHz

- **16-Bit timer overflow results in:**
  - Software reset
  - Pulls RSTOUT Pin low
  - Sets identification bit and leaves WDT enabled
- **Programmable input clock**
- **High Byte reload register**
- **Timer period from 25.6µs to 470ms**
- **Can be reloaded with a special instruction**

C161
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WDT
Block Diagram

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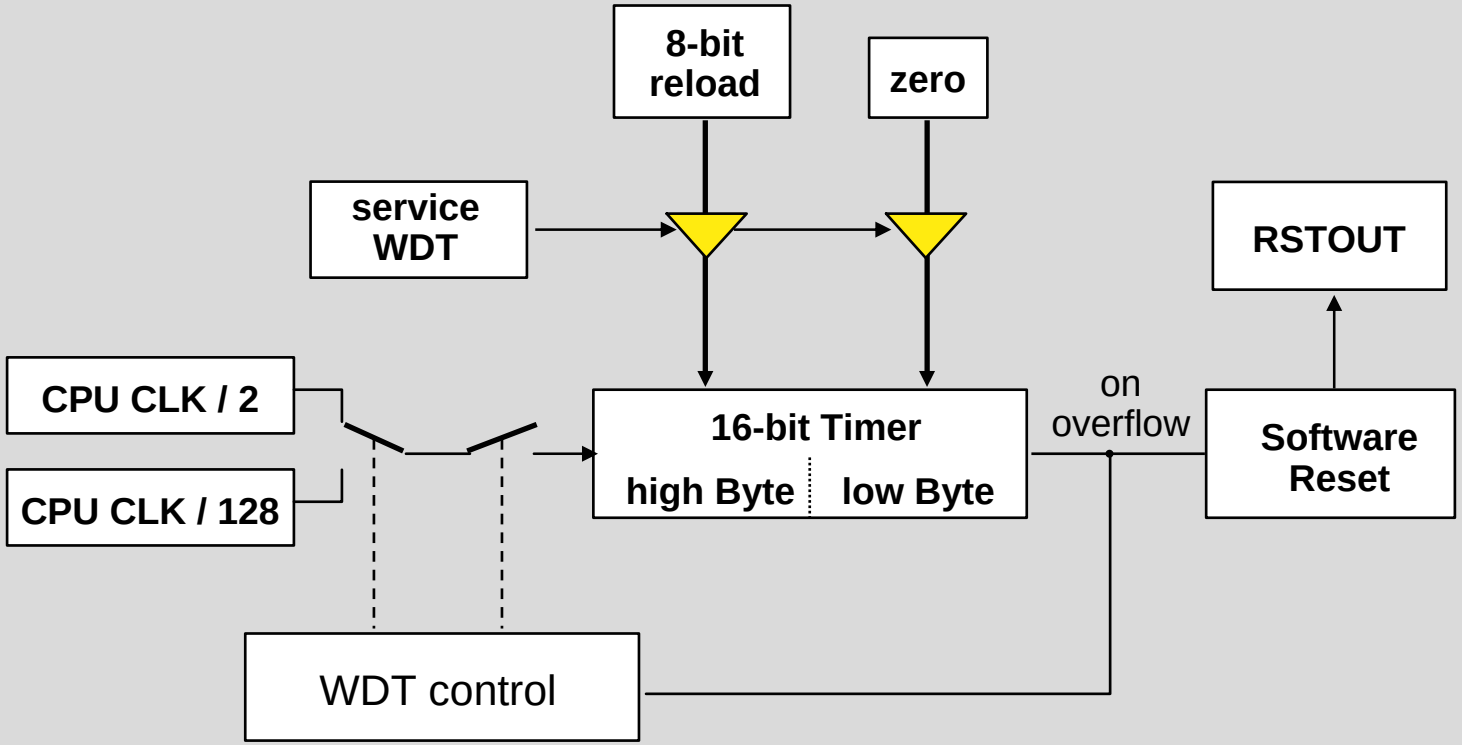

Overview Port Structure

- **The Port lines provide the connection to the external world**
  - 77 Port lines on the SAB 80C166
  - 111 Port lines on the C167
  - 77 Port lines on the C165/C163
  - 59 Port lines on the C164
  - 64 Port lines on the C161V/K/O
  - 77 Port lines on the C161RI
- **All Port lines are individually addressable and all I/0 lines are independently programmable for input or output**
- **Each Port line is dedicated to one or more peripheral functions**
- **Each Port is protected with fast diodes**
- **Programmable open drain buffers**
  - P2, 3, 6, 7, 8 on the C167
  - P3, 8 on the C164

C161
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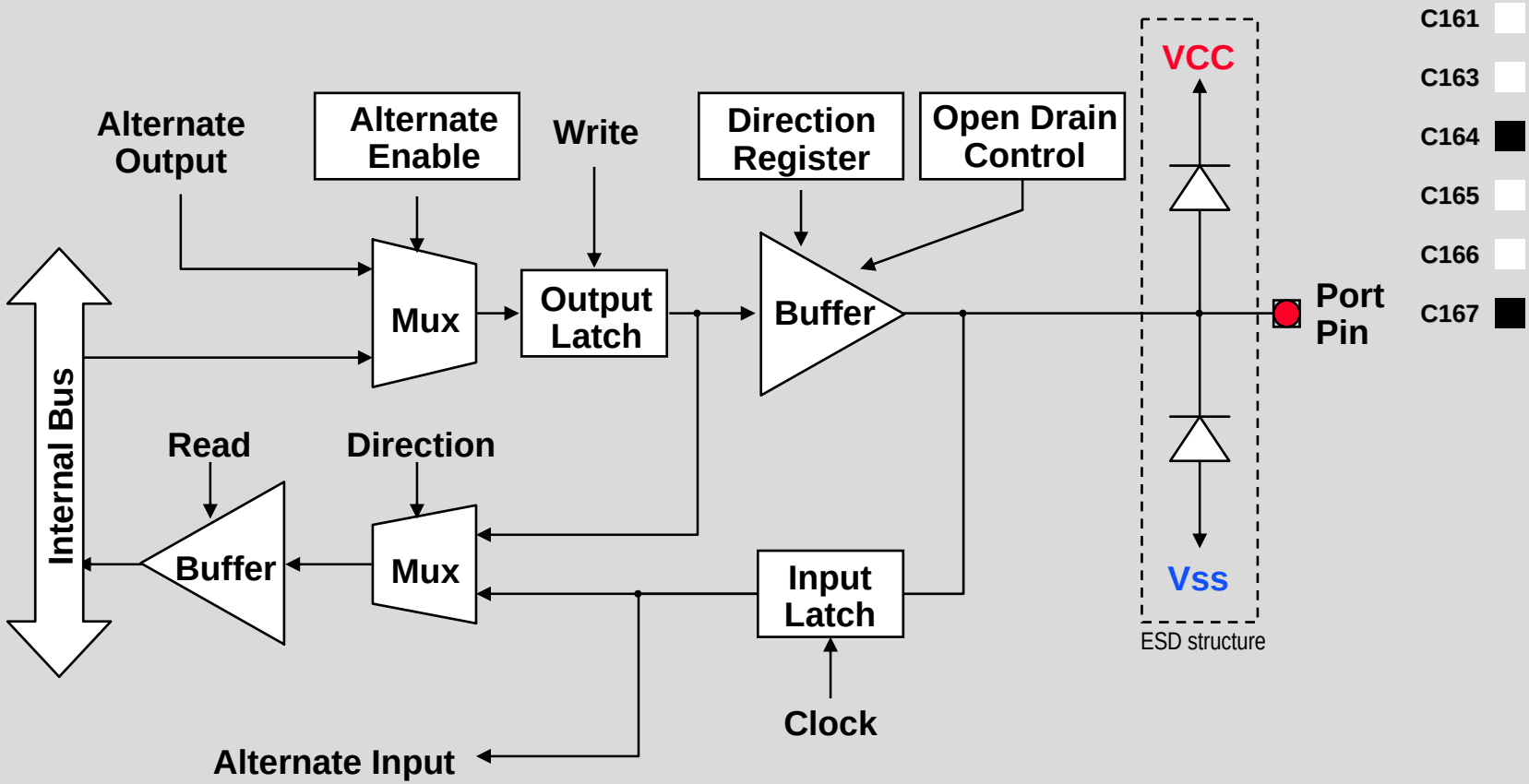
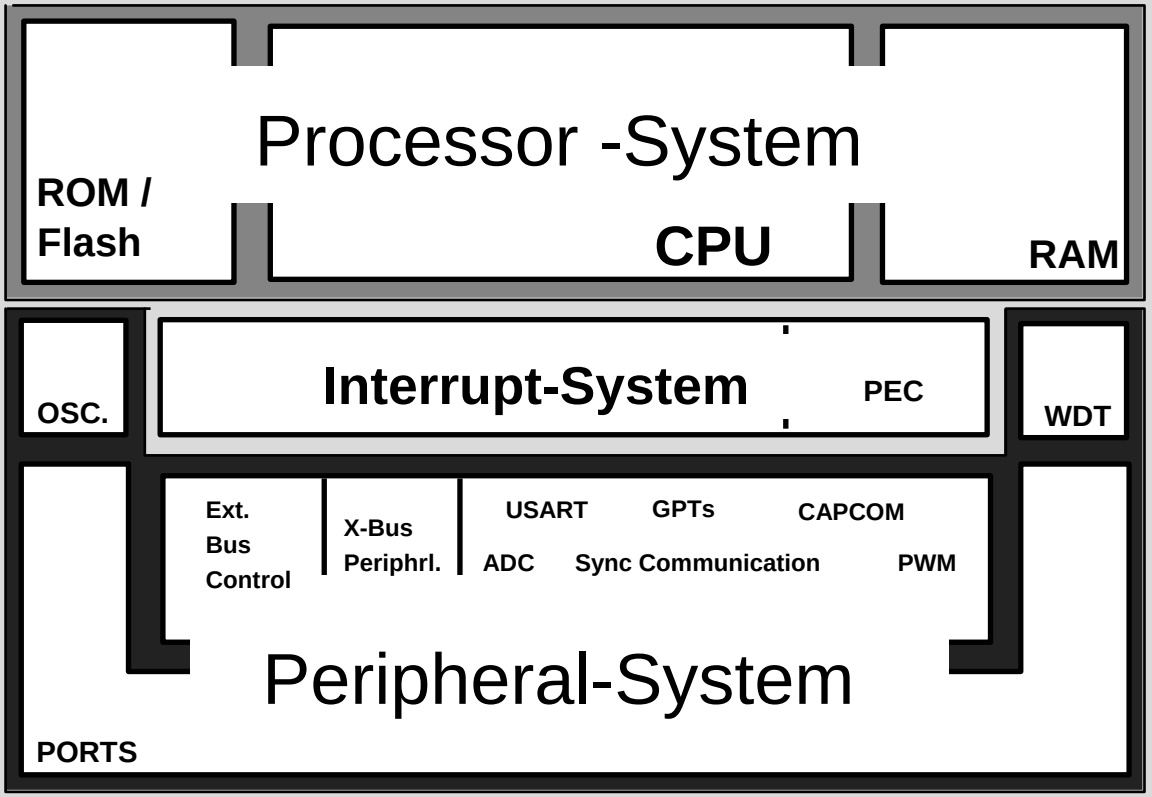
Overview Port Structure



The Summary of the C166 Family



- C161
- C163
- C164
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- C166
- C167

Processor System

- **High Computational Power: min 80ns Instruction Cycle Time**
  - Fast algorithms (short sample times for closed loop control)
  - Fast task execution
- **Control Oriented Instruction Set**
  - Boolean processing / bit-handling and processing
  - Task switch / power saving
- **General Purpose Register Oriented Architecture**
  - Managing of multiple quasi-parallel tasks
- **Powerful Addressing Capabilities**
  - Large address range and powerful addressing modes (HLL)
- **On-chip RAM, OTP/ROM/Flash**
  - For very fast Memory Access
  - In-System reprogrammable Flash Memory
  - one-time programmable ROM

C161
C163
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Interrupt System

- **Extremely Short Interrupt Response Time of typically min. 320ns**
  - Interrupt execution in small time segments
  - Ensures highest real-time performance
- **Comprehensive Prioritization Scheme**
  - Easy scheduling of complex real-time systems by using up to 64 Priority levels (4 groups within 16 levels)
- **CPU-Independent Interrupt Service via Peripheral Events Controller (PEC)**
  - Off-loads the CPU from simple but frequent interrupt-services
  - Interrupt-driven “DMA-like” data transfer, without task switch of CPU
  - Makes peripheral data transfers independent of running CPU routine

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Peripheral System

- Multi-functional Timer/Counter Units (up to 5 Timers / Counters) with Complex Concatenation Possible
- Comprehensive up tp 32 Channel Capture/Compare Unit with up to 4 Allocatable Time-Bases
- Capture/Compare unit (CAPCOM6) for flexible PWM Signal Generation
- 4 high resolution PWM channels
- up to 10-bit Multi-Functional A/D-Converter for Fast Data Acquisition in Control Systems

C161 ■
C163 ■
C164 ■
C165 ■
C166 ■
C167 ■

Peripheral System

- **Bi-directional, Protected and Individually Programmable External Port-Lines**
- **Serial Communication Interfaces**
  - Standard asynchronous communication
  - Fast synchronous communication in master- & slave-mode (SPI)
- **Easy Adaptation to Special Application or Customer Requirements via Internal X-BUS Architecture**
  - CAN-Bus, Profibus, SSP, etc.
- **flexible Power Management**

C161
C163
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2-chip Emulation Technology

- One Bondout chip supports emulation of all related derivatives, new or existing (i.e. C167, C165, C163, C161)
- New X-Peripherals (XPERs) are emulated using the standard chip
- In emulation mode the standard IC is sleeping and only the XPER is active. The Bondout chip has full access to the XPER over a particular port
- No need for Bondout redesign
- User has full emulation control over the XPER without any intrusion of real-time
- Full access to target system is maintained
- Supported by all major tool manufacturers

C161 ■
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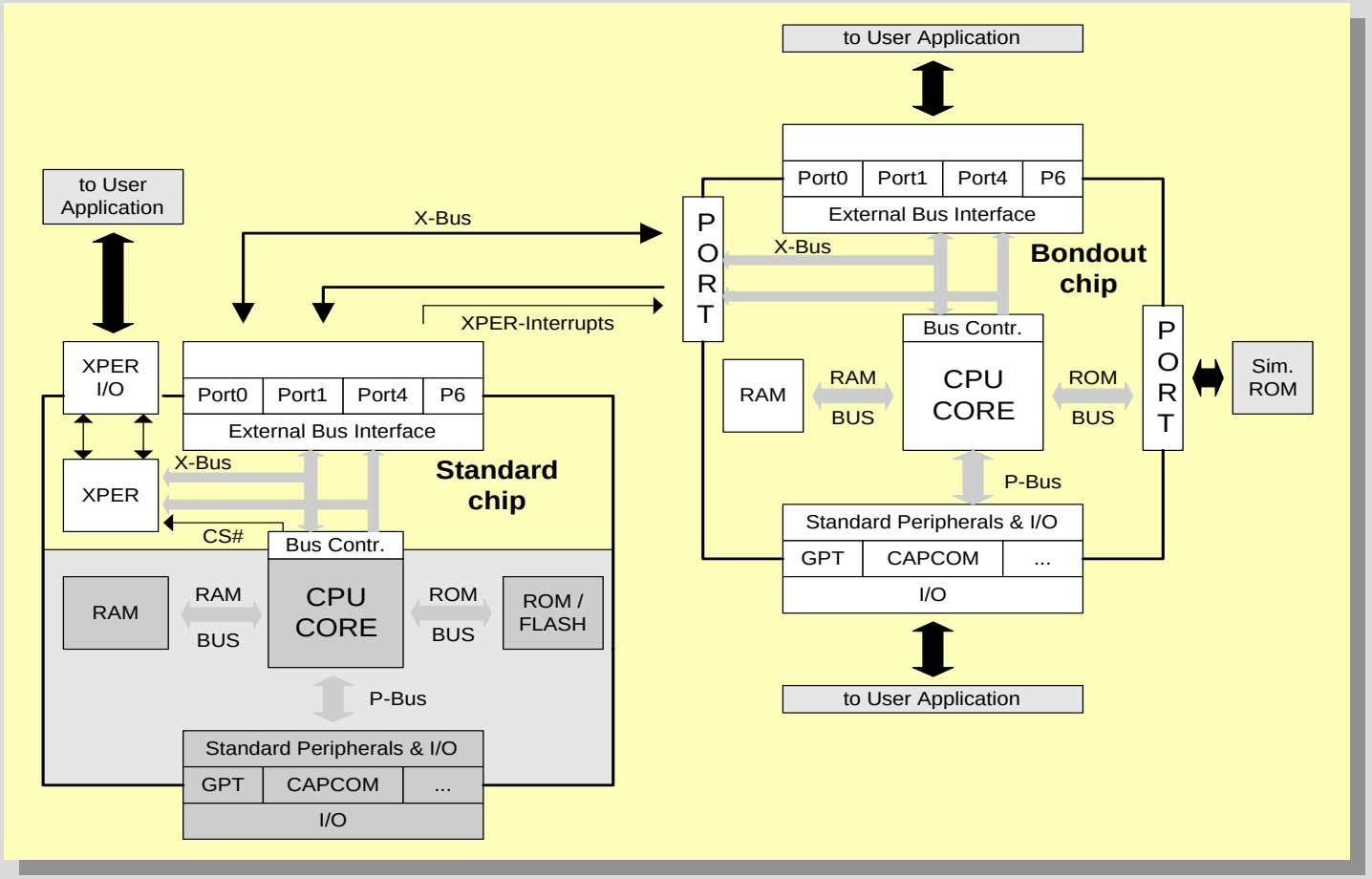
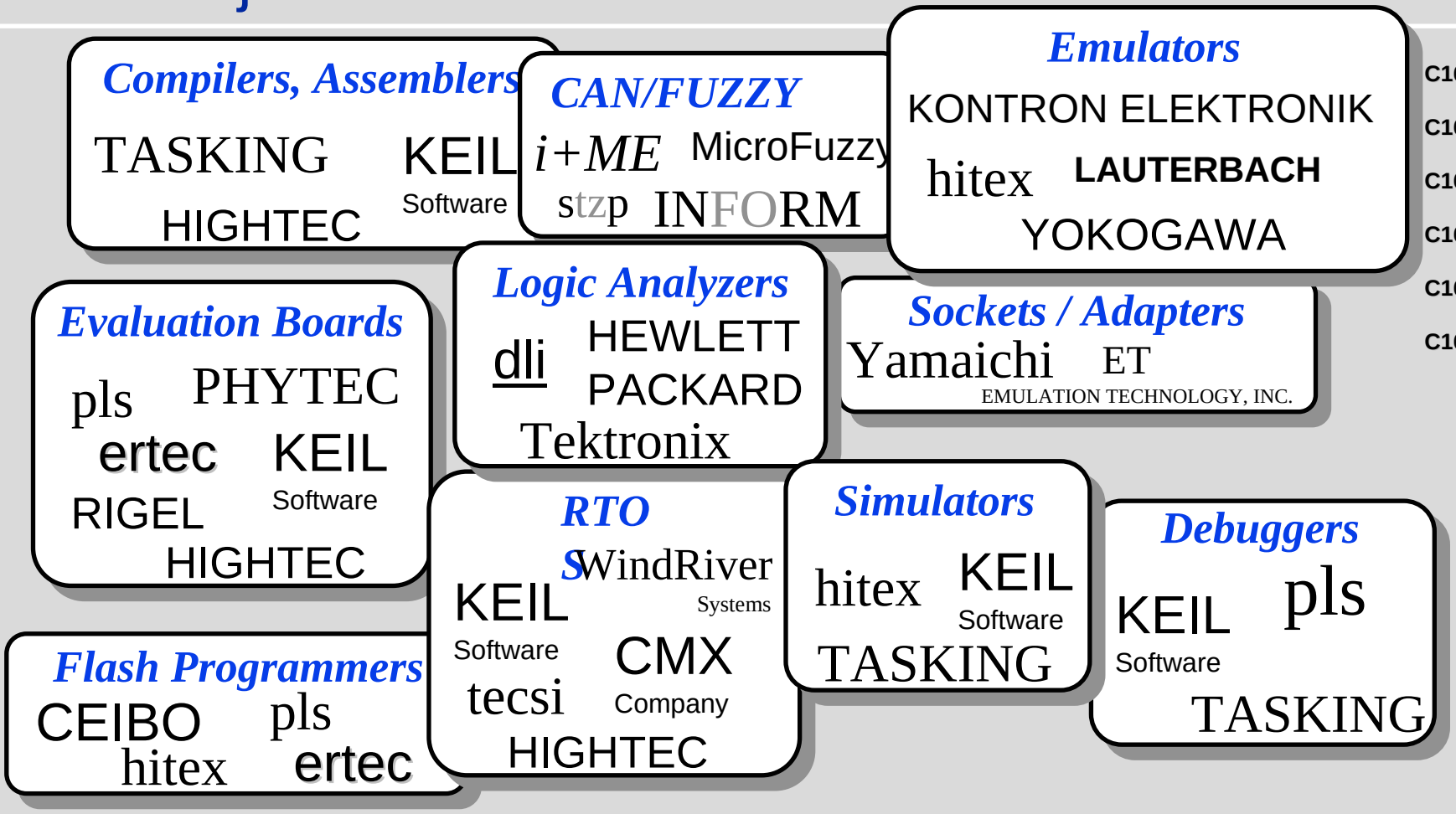
C166 □
C167 ■

2-chip Emulation Technology



C161
C163
C164
C165
C166
C167

Major Tool Partners



C161
C163
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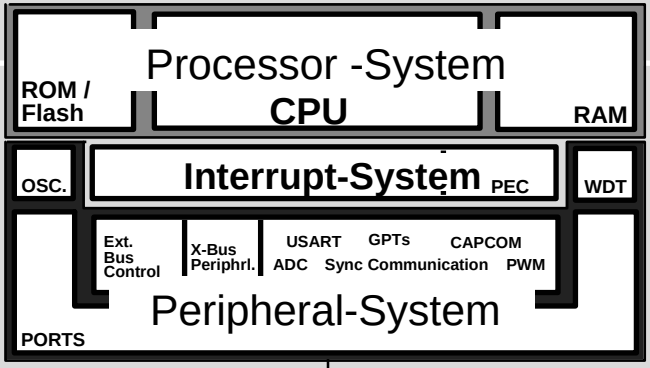
C166
C167

Applications for the C166 Family



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C167

Automotive	Industrial Control	Consumer	Telecom/ Datacom	EDP
• Engine Management • Transmission Control • ABS/ASK • Active Suspension	• Robotics • PLC's • Servo-Drives • Motor Control • Power-Inverters • Machine-Tool Control (CNC)	• DVD / CD-ROM • TV / Monitor • VCR / Sat Receiver • Set Top Box • Games • Video Surveillance	• Communication Boards (LAN) • Modems • PBX • Mobile Communication	• Hard Disk Drives • Tape Drives • Printers • Scanners • Digital Copiers • FAX Machines